The Schottky CMOS (SCMOS) – The densest IC technology and circuit embodiments for the 5thG microelectronics. A. Chang, 10/10/2004, GSD Confidential

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The Schottky CMOS (SCMOS) Technology – The densest analog, logic, and memory circuits for tomorrow's microelectronics. Oct. 7, 2004. Augustine Chang, Golden Silicon Designs, gus@goldensilicondesigns.com, Member, IEEE.

1. Background review.

In the pursuit of advancing microelectronics circuit implementations over the past 5 decades, industry has been in search of the means to provide higher and higher integration density and functionality. Innovative process methods, device structures, and circuit configurations have propelled evolutionary and revolutionary improvements from generation to generation of integrated circuits (IC).

Useful IC products appeared in the market starting from small scale integration (SSI) in the 1960s, to large scale integration (LSI) in the 1970s, to very large scale integration (VLSI) in the 1980s, to ultra large scale integration (ULSI) in the 1990s, and finally, to Super Large Scale lntegration (SLSI) in this decade. In keeping with the famous Moore's Law, we observe that density has doubled every 2-3 years for the past 5 decades. The productivity gains were attributed to the underlying technology – solutions based on the combination of process, device, and circuit advances. We have been relying on continuous, innovative ideas and breakthroughs that have paved advanced technologies in hardware miniaturization with embedded software. The technology introduced lower cost performance solutions such as Bipolar RTL, DTL, TTL, ECL before 1980. FET work in PMOS, NMOS, BiCMOS, CMOS began in 1970 and has matured in the last decade.

In this article, we shall describe an emerging technique called Schottky CMOS(SCMOS) as a new paradigm for boosting the drive of mixed signal low power IC solutions in a system on a chip (SOC) environment.

2. The AAPY bench mark index and field programmable IC.

Throughout the various IC technology generations, there are four well known benchmark matrices that measure cost-performance figures at final chip and printed circuit board (PCB) product levels. These cost-performance measures which include physical area, access speed, power consumption and efficiency, and device yield (AAPY), may serve as a direct chip productivity index (CPI), governing the figure of merits of an IC technology and its packaging constraints. The fifth critical factor is the instantaneous programming or reuse capability of on chip resources and functions in a device. The reasons are quite simple: not only does this eliminate expensive process alteration, but it adds unlimited SW integration, circuit functional controls, and wiring flexibility to the end devices.

Generally speaking, the device and its package are simple and less capable, reasons against full integration. Many designers consider aspects of the CPI stressing one or two dimensions separately instead of the stressing multiple dimensions together. There is a

broad range of stand alone logic devices that emphasize speed only; there are memory devices that emphasize density; and there are mobile ICs that emphasize power savings. The analog and digital IC each finds its own market space. However, for a winning technology in the SLSI era, one needs to tackle all factors as a whole, so as to combine all advantages into one SOC unit —underpinned by superchip technology.

Low barrier Schotttky CMOS (SCMOS) and Schotttky CMOS Logic (SCL), made with a new diode element , simple circuit configuration, and stacked metal wiring planes, possess the following attributes:

- reduces driving point RC time constants;
- reduces three terminal transistor counts (replacing transistors with diodes);
- reduces gate counts;
- reduces wiring tracks in lower metals;
- reduces cell pitch sizes and wiring distances;
- reduces ac power and peak current;
- reduces switching node counts;
- reduces signal swings;
- reduces parasitic pocket counts, and capacitances;
- reduces ac power consumption;
- reduces access times in all types of circuits;
- reduces defect areas per circuit unit;
- supports wide range of analog functions including ESD protection, latch up prevention, clipping, clamping, rectifier and class B amplifications;
- supports online and offline reconfigurations;
- downward compatible with conventional CMOS libraries;
- may be integrated with multi-level Flash transistors.

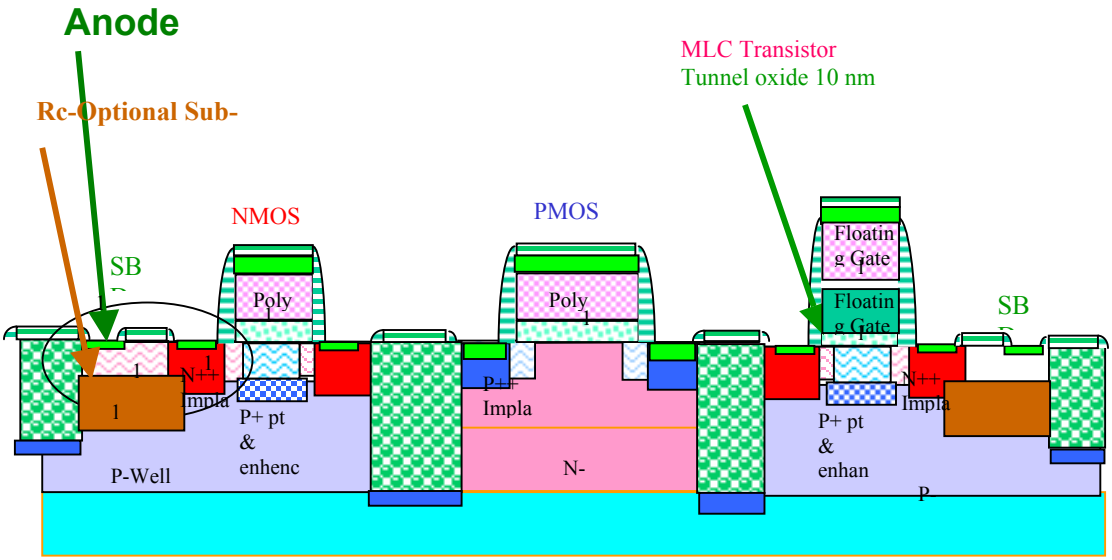
SCMOS and SCL therefore offers a superchip paradigm with the densest analog, logic and memory (ALM) units. The combined superchip scheme supports universal IC chips (UIC), processors with abundant storage, and memory devices with programmable intelligence.

With embedded soft and hard coded macros, we shall cross the classical boundaries between analog and digital chips. One can seek an ideal physical layer for device integration which can contain as many as possible various circuit elements of R,L,C, and transistors in a single chip. Useful HW/SW constructs shall support target implementations that exhibit large capacity, dynamic functionality, field programmability, and acceptable power consumption. These features are commonly supported with new SCMOS devices.

3. Process, device profile, and circuit configurations of SCMOS

Fig. 1 below shows a cross sectional view of a SCMOS device. Oxide trenches isolate the Schottky Barrier Diode, NMOS, PMOS, and Flash transistors. Standard passive circuit

elements such as metal inductors, poly resistors, capacitors, and thin film metal capactors, are not shown.



Standard processes: Conventional Trench/ROX Isolation, CMOS transistors, and post contact metal processes

Fig. 1 Cross sectional view of integrated SBD, CMOS transistor, and Flash transistor.

Conceptually, the SBD is of low turn-on threshold and is formed by refractive metals alloyed with Si crystals in the near surface region. The atomic metal work function and the conduction energy band of the semiconductor determines the barrier heights and govern the built-in voltage barrier which prevents electron flow between the metal film and silicide compound layer. We will address the current transport model later.

The regular NMOS and PMOS transistors are fabricated by their standard process flows. In certain applications, we can integrate Flash transistors as storage memory units. It is conceivable that an SBD may be integrated into any of the transistor beds to share source/drain contacts. An SBD so constructed may be of P-type or N-type respectively if it merges with PMOS or NMOS transistors. In the illustration, the SBD is of the N-type. It has an Anode contact at the barrier metal compound. The cathode body is buried in the Si bulk. The cathode resistances are controllable by the width and length of the diode design and an optional ion implant region. The physical difference between an SBD and source-drain contacts lies in the blocked out N++ implant diffusion for the anode. Similarly, a P-type SBD may be formed in the P-MOS source-drain region where the metal film becomes the cathode and the Si body is the anode.

4. The theoretical electrical device model

The equation below describes the 1st order thermal ionic forward I_V curves,

$J_T=R(T+273)^2*EXP(-q*Vb/(K*(T+273)))$ (1)

$I_T=A*J_T*(EXP(qVF/(K*(T+273))))$ (2)

Where J_T and I_T are current density and current load of the forward diode, R is the Richardson constant, T in kelvin, K the botzman constant, Vb the barrier height in eV. The I-V characteristics of a typical SBD is illustrated in Fig. 2 below.

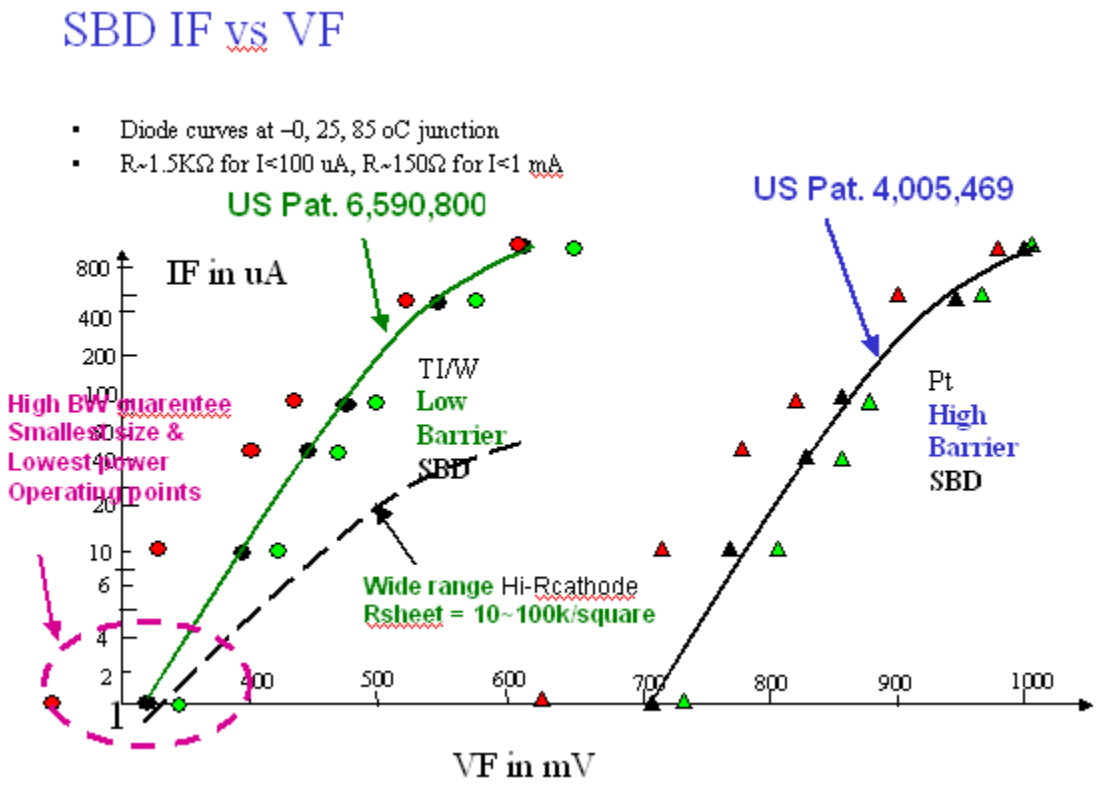


Fig. 2 Low barrier and Hi barrier SBD forward comparison

Earlier work by this author in the 1970s produced curves using Pt or Al metal compound and is shown in the curve to the right. More recent work using Ti, Co, Ni, Pd may yield the low barrier diode curve which is shown on the left. The leakage current under reverse conditions may be contained under 1-10 nA range via careful engineering control by process conditions for a submicron device, say 0.18x0.18 um in size.

5. Basic logic circuits

Many patent pending device applications are pursued using the newly added low threshold diode element to implement random logic, analog, and memory functions. In many situations, by omitting the isolation terminals in a simplified physical layout, we may use the simple 2-terminal diode to replace the bulky 3-terminal transistors in delivering the desired functions more efficiently. An exemplary NOR gate consists of

asynchronous clock pulses biasing an OR logic diode tree which is closely coupled to a simple CMOS inverter(s). This is shown in Fig. 3(left) as a typical Schottky CMOS Logic (SCL) implementation. Compared with a counter part NAND (or NOR not shown) gate using conventional CMOS transistor to transistor logic (CMOS-TTL), one may quickly observe important differences.

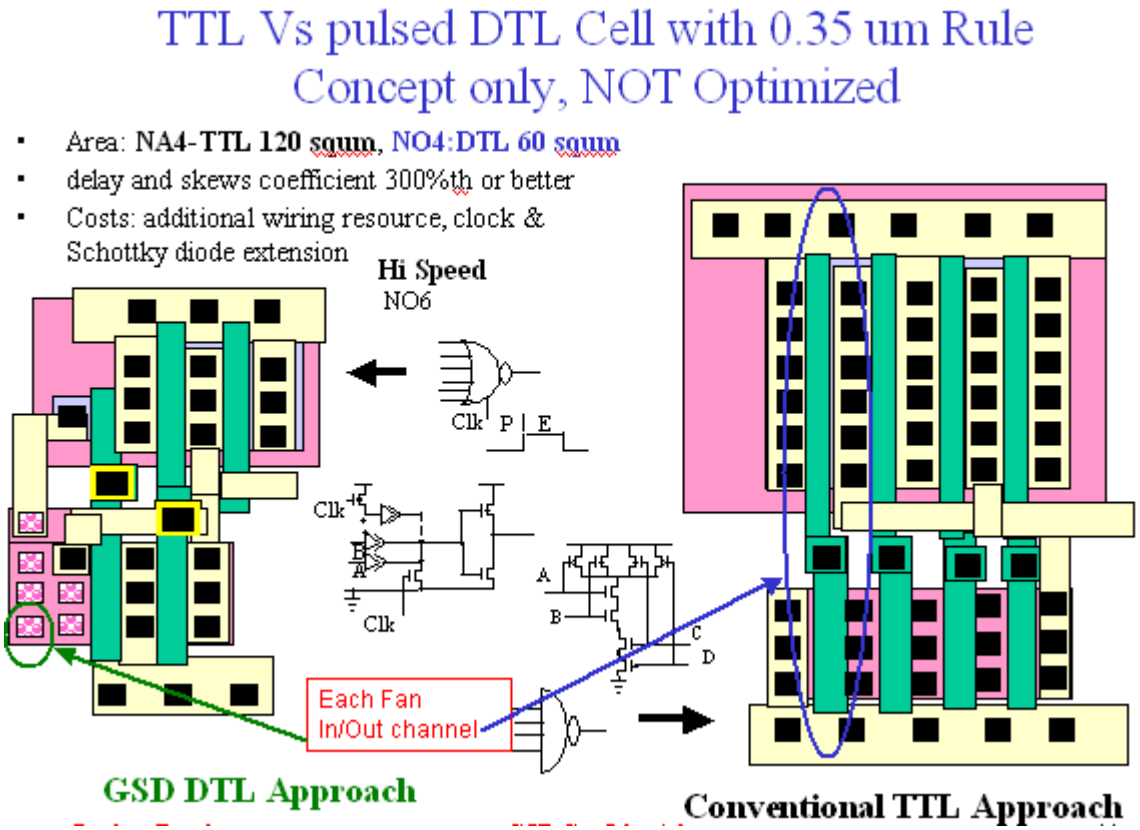


Fig. 3 SCL and TTL circuit comparison

1). The physical construct of SCL is significantly smaller than the CMOS-TTL logic.
2). The circuit configuration of SCL gate is much simplified compared with the CMOS-TTL logic.

There are important attributes derived from these physical and circuit merits. The SCL circuit has only one primary internal switching node since all diodes share the same s/d node of the clock biasing transistor. The TTL circuit, however, during the down switching edge, turns on all of the s/d nodes over 4 transistor pockets serially in the N-leg and 4 more bulkier parallel transistors pockets in the P-legs. Each of the TTL circuits suffers with either N-leg or P-leg serial transistors that add up to large time constants and switching delays, and draw more ac power or ac transient current. Further, the load of TTL interfaces, which are governed by the wiring width and length, and gate-pair capacitances, are aggravated by the cell's inherently larger pitch, longer metal runs, and poor fanin*fanout products.

The circuit switching controls of SCL are much easier to optimize. Dependent on the phase of clock signal, the SCL switching windows are cranked to be either in a precharge mode or in a evaluation mode. During the precharge mode, one of the internal diode asserts a clamping function to the 1st stage inverter, forcing it to stay in either of the dc rail levels; therefore, it is logically disabled, drawing almost no subthreshold current (assume Vtt=0.5V, Vtd=0.1V). During the evaluation window, logic functions are valid in each unit in the path. Signals pass through the invertors and combinatorial chains, finally latched by the clock in the respective CMOS latch/DFF units. The AAP index is optimized, since gate, transistor, and internal node counts are reduced, parasitic capacitances are small, fan out is larger, and fan in is wider. In standard cell like logic array units, one can realize any complex function with place and wire CAD software by reconfiguring intra and inter circuit units from designated basic library cells of softmacros and optimized hardward blocks. To maximize chip space and speed benefits, we may save horizontal wiring track spaces by trading off stacked tracks in the vertical dimension with stacked metal planes (up to 8 layers now supported). Furthermore, since current levels are reduced by orders of magnitude, the wiring metal can be thinner and narrower, greatly improving metal delay.

The advantages of the SCL type cells include but are not limited to:

- densest physical sizes of ALM/UIC circuits in Si wafers;
- lower supply voltage, ac currents, and ac power for all ALM circuit types;
- fastest switching RC time constants in least switching node(s);
- downward compatible with CMOS-TTL type cells;
- wider Fan-in, more Fan-out per gate;
- least gate counts;
- least transistors counts;
- least nets counts;
- best ALM unit integration;
- best device yield in Si wafers.

Lab data shows the SDB having a forward switch on voltage of around 0.1 volts while conducting from 0 to the mili-ampere range. Reverse saturation current is capped at under 1 nA.

In the precharge window, the capacitive load is blocked by the off state diode, and in the evaluation window, the driver sees the 1st stage inverter gate-pair of the receivers. So the driving power of SCL circuits is also significantly better than its TTL counter parts. Fig. 4 shows a benchmark comparison of the simulated combinatorial logic gate speed versus gate-pair loads. It shows significantly better speed performance for the SCL circuits compared to the TTL circuits.

While delay variance limits TTL circuits to less than 4-way fanin and 3 gate-pair loads, we are encouraging designers to use wider SCL fan-in gates for decoders and muxers to realize more AAPY benefits. The inverter may easily drive an enormous number of SCL receivers.

SCL may concurrently support both interface signal types of SCL and TTL. Since SCL is operated on dynamic pulsed logic, one should latch the result in a simple TTL latch or DFF cell. A general guideline is to employ no more than 2-way TTL cells. This strategy resolves the circuit compatibility issue and lets the user picks the best part of the circuit types. Note that the best performance interface units is SCL cells driving SCL cells with customized wiring tracks in a multilayer wiring planes using the narrowest metal tracks.

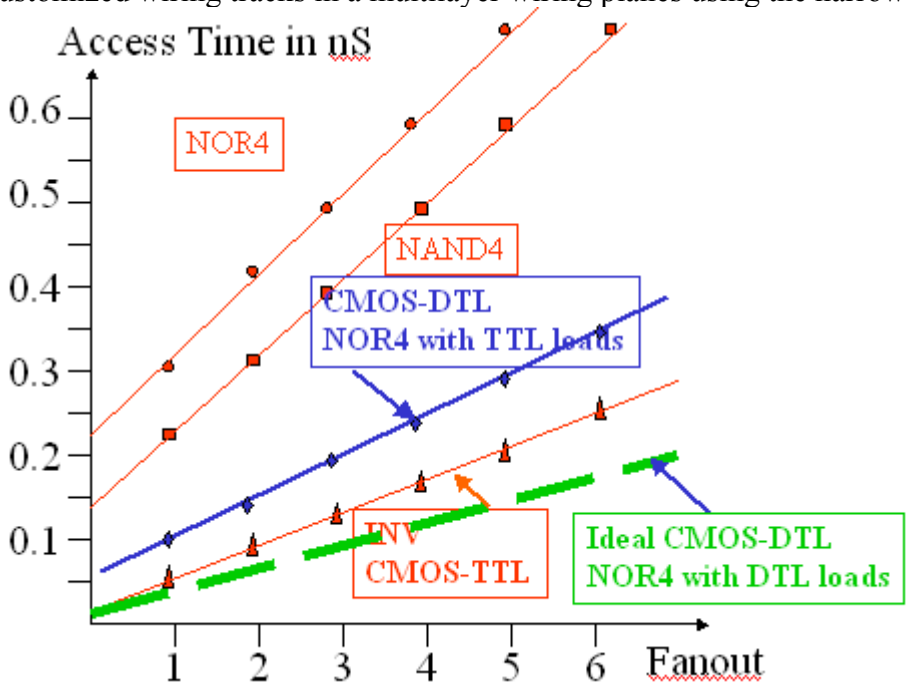


Fig. 4 Speed bench mark curves of SCL and TTL circuits

Since each of the fan-in signal channel only costs an anode contact of the bulk area, SCL becomes the densest logic circuits in any of the Si technologies known to date.

If we accommodate 8 layers of wiring planes, we may implement the densest, fastest, and least power consumption IC circuits with SCL constructs. Furthermore, since it has wider fan-in, lower loading, and smaller cell pitch sizes, SCL actually reduces gate and transistor counts in chips, thus reducing cost and increasing device yield. Since SCL are basic circuit units, this design approach may improve the AAPY index of many memory and analog peripheral circuit units.

Each of the SCL circuit unit(s) may provide dual sets of signal interface points. One set is TTL, which comes out of transistor S/D contact directly. The signal swing is rail-to-rail.. The other set has diode drop offset(s) in 0.1 steps or higher from either power or ground. Additional signal levels can be supported by diode offsets when needed and properly justified.

6. SCL leakage stop and controls

Referring to Fig. 3 circuit schematics, the active clock transistor also serves as the biasing leg in active mode (E window). The clamped internal node may have power-speed trade-offs. While the inverter transistors are short channel devices, the clock transistors may employ a narrow width device for the least biasing currents.

To contain the leakage current level of the reversed diodes during precharge mode, there are several device and circuit measures. Firstly, if the chip is of low speed class, we may insert large cathode/anode resistances. The undoped or lightly doped Si resistor body may easily be designed in the mega-ohm range. Secondly, we study failure modes and reduce the defects in the peripheral and metal compound region. This may require detail process procedures, treatments and conditions in fine tuning the barrier metal deposition, thermal treatment, and etching procedures. The third circuit level solution is to add a leakage stop MOS transistor in the driver path. This is shown in Fig. 5. for the case in NOR gate. The circuit operation concept is explained below.

During the P-window, node 1 is pulled high, and the NOR gate is dc statically clamped. The inverter does not care about input logic but its output is at GND level. The diode input states are all ignored except for leakage concerns. If the diode input is asserted down, the SBD is stressed by the driver of its previous cell. We can use a cell type with a leakage stop, ie. The NMOS transistor Tlsn in its N-leg. Clkb controls Tlsn to disable the leakage path during P-phase. No Tlsp is needed there. During the E-window, Tlsn is asserted. It does have a slow down effect but is acceptable for 2 stack N short channel devices.

Like wise, Tlsp may be added to the previous stage SCL cells for NAND critical cells. Since all circuits are operated by the same clock buses, SCL cells with Tlsn or Tlsp may be grouped together by a common pair of transistors. Therefore, the physical size and speed impact in leakage stop facility becomes trivial and affordable.

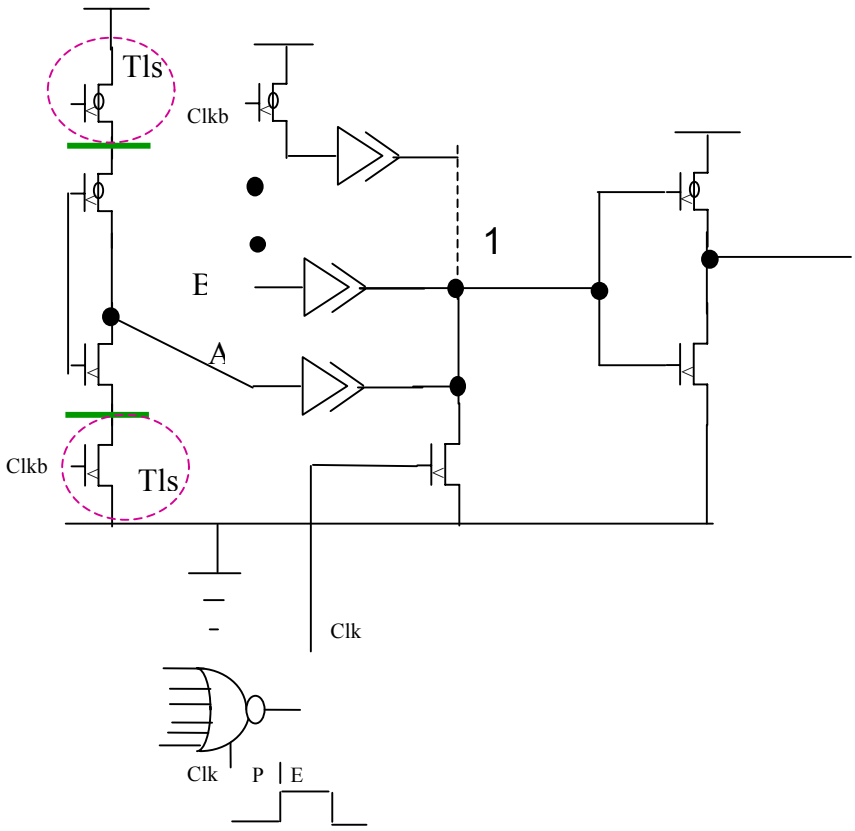
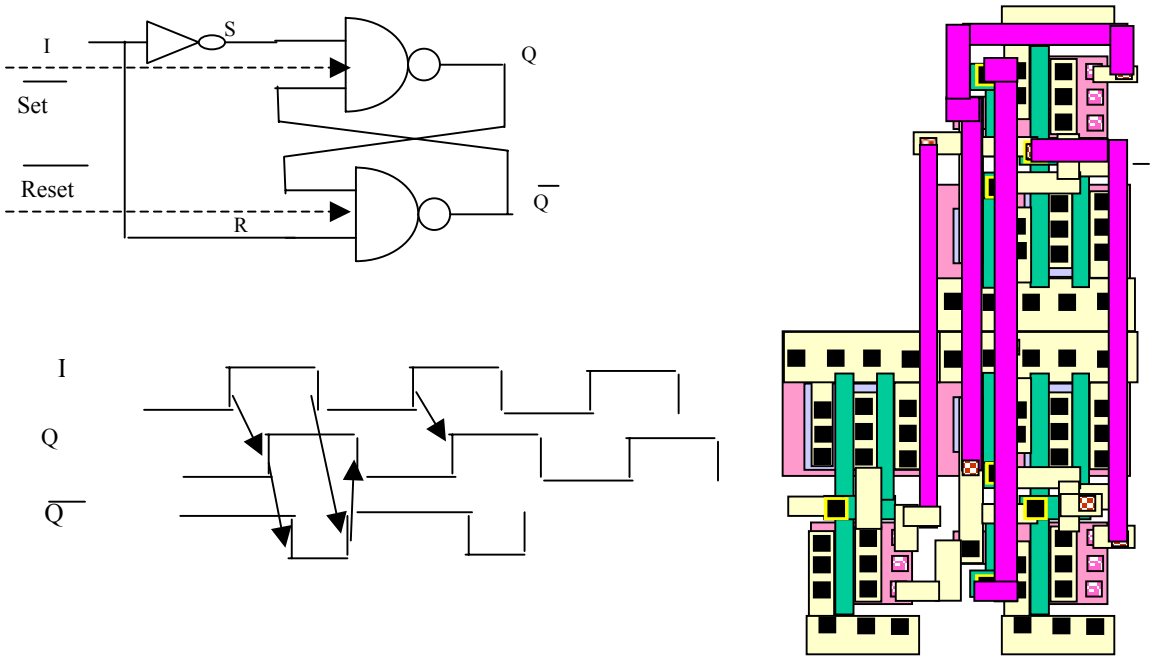


Fig. 5 Leakage stop means for critical SCL circuits

7. Extensive Aanalog, Logic, RAM, and ROM applications

SCL and SBD may be used extensively as basic building blocks to implement complex ALM functions, schmitt trigger, timers, converters, clippers, ladders, encoders, decoders, data path, embedded memory cores, PLA, ROM, OTP or mask ROM, FPGA, EEPROM, and others. There are several examplary hardward constructs cited in US patent 6,590,800, and more are patent pending. In this section, we will review design concepts of several constructs, but leave out detail optimizations.

Fig. 6 shows a sea of gates type standard cell wiring scheme. The optimized layout shall consume as little horizontal tracks in M1 layer as possible but stack tracks in higher metal layer wiring planes. Thus, all intercell wiring are at minimum Manhattan distances. Since the SCL circuit has lower current levels than TTL, all traces may have more aggressive scaled down physical geometries, which also result highest wiring capacitance.



The Fig. 6 sea of gates dynamic DFF implementations.

Fig. 7 show a 4Tx SRAM cell circuit (US patent 6,590,800) in comparison with the conventional 6Tx cells. The 4Tx cell arrays operate on voltage mode switching principle. Twin word lines replaced the power rails. The cell pitch saves 30% since the pass transistors are replaced by SBD. The bit lines are 30% shorter and SBD blocked all cell internal node capacitances. All bus signals swing only ½ VDD for speed, power savings, and noise margin reasons. SCL blocks are used in all peripheral cross sections for high density, high speed, and low power operation.

SBD, which are highly conductive and have the exteremly low parasitic capacitance, are ideal for high speed RF input nets, ESD protection, and latch up protection. The SCL super cell library further includes applications in Schmitt trigger cells, timers, image sensors, op amps, band filters, Sigma Delta converters, and PLL/DLL circuitry which may be designed to operate with a 1.2V or less rechargeable battery.

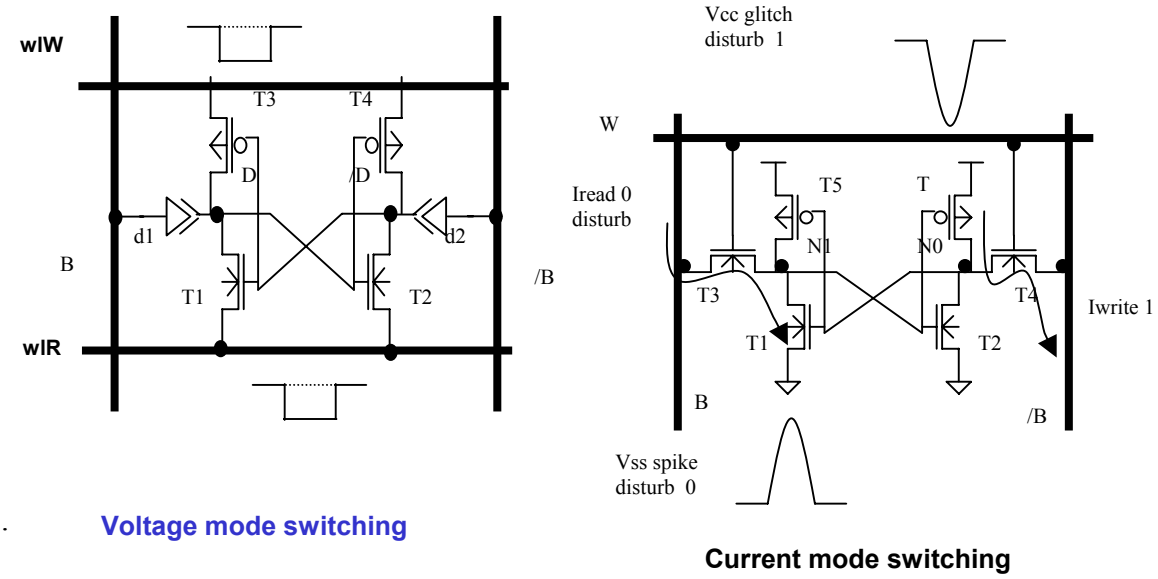


Fig. 7 The 4Tx and 6Tx SRAM cells.

8. SCL may mix with Flash transistor and may be used in SiGe circuits

We have patent pending applications incorporating low barrier SBD to serve other critical functions. The SCL is the densest, fastest, and least power logic circuit implementation in Si. It can be adopted to improve all analog ,memory control, and peripheral hardware for AAPY enhancements. Since a Flash device with multilevel cells (MLC) is currently the densest storage unit, integration with SCL will result in the ideal SOC solution. We are also pursing SCL-based FPGA (SFPGA) techniques.

One of the proposed embodiments uses the Flash transistor (N or P types) to replace the NMOS(or PMOS) SCL inverter. Hence, the SCL gate may be used as an AC analog comparator which directly read out multilevel signals. It may communicate with MLC directly, simplifying the signal translation process. Since SCL is very simple in circuit topology, it can be easily and extensively programmed and erased on the fly to store commands or procedure codes. Dedicated resources which change transistor thresholds of selective units can be designed to decode and reconfigure softmacros to perform active or passive functions, and to complete intra and intercell wiring. We can alter online, predefined, critical basic and large circuit units, change impedance termination schemes, and enable or disable critical controls. In many situations the ADC/DAC conversions are more efficient, and the data processing delays are shortened.

In the mixed signal environment of various ALM units in the UIC, all functions are delivered by the most efficient units of local embedded blocks. Efficient controllers may be implemented to integrate processor and storage functions. SCL and Flash superchips may contain the densest logic and memory blocks. The UIC may be either logic intensive or memory intensive, but are certainly greatly enhanced in AAPY index. They may

incorporate various large embedded arrays, special functional units, fixed or softmacros, and analog and digital blocks.

The UIC devices may perform highly complex operations, responding to protocol and command changes. They may perform ternary or quaternary logic in certain internal units and bus interfaces. System computing resources are modular and distributive. Regardless of whether the nets are on chip or off chip, their data rate limits are pushed to much higher. They may vary, and should be adaptive to physical environments. Controller functions are pushed down from board level; they may either reside on chip, or on mini cards closer to memory (DIMM for instance) or storage chips (USB disk sticks or MultiMedia Cards) in the same subassembly.

The subassembly is powerful and controls both high level commands with simplified physical interfaces such as USB, wireless phones, fully buffered DIMM, and low level bus lines within the chip or small PCB. All functions can be altered or reconfigured while portions of the chip are hot and alive. Many cases use single chip devices delivering full ALM system functions. Computing power is distributive and accumulates as more devices are daisy chained.

Similar to connecting diode logic trees to a CMOS inverter in SCMOS, there are schemes that diode trees may couple with bipolar buffers in super high speed SiGe chips. This is the situation of Schottky with hetero Bipolar Transistor (SHBT) where SBDs are incorporated into lightly doped epi layer wells/beds. The advantages here include space savings, high power and high Ft. The drawbacks include DC current and device yield costs, which is inherent with SiGe wafers. However, SHBT schemes may offer HBT with certain relief and optimizing AAPY figures in a way that is similar to what SCL offers CMOS-TTL.

9. Summary

Table 1 summarizes CPI statistics of IC implementations over 50 years.
Table 2 summarizes IC design parameters over 50 years.
The industrial CMOS/Bipolar technology cross-over occurred in the 1985 time frame.
We believe the CMOS-TTL drive will meet stiff resistance for the arguments discussed in this paper.

We anticipate that SCMOS, SCL, Sflash, and SFPGA design platforms will move into the center stage in the 5th generation of IC technology for its cost effective attributes and desirable features.

In conclusion, we yield the following trends and observations:

- The low barrier SBD is an ideal new circuit element to offer low power, low voltage, low current circuit switching.
- SCL is attractive because it reduces transistor and gate counts. It supports the continuing physical and electrical scaling of ICs.
- SCMOS and SCL are much more cost effective than CMOS-TTL, yet downward compatible with CMOS-TTL.
- Sflash and other memory devices can be improved by incorporating SCL cells and controls.
- SFPGA is an attractive and integratable product feature; and it is doable with SCL.
- Mixed signal analog, logic, and memory implementations are the trend; UIC and distributive computing may be deployed with SFPGA and embedded cores.

Table 1, IC circuit solution and cost trends

Figure of merit index (AAPY) comparison on NAND4 gate

		Area	Access	Power	Defect	AAP
	time	Weighted Cost Factors				Total
Bipolar TTL	1980	100	100	100	100	1E8
Bipolar ECL	1985	200	10	200	200	8E7
CMOS TTL	2000	10	10	10	10	1E4
CMOS-SCL	2004	2	2	2	2	16

Table I1, IC circuit design parameter trends

	Bipolar		CMOS		
Tech rules/pars	1970	1980	1990	2000	2 010
Gox/Wb Ang	4000	1000	200	70	30
H um leff	6	3	1	0.25	0.07
H um film	1	0.5	0.4	0.3	0.1
Contact/space um	10	2	1.2	0.25	0.1
Typ C load in F	10pF	1pF	0.4pF	200fF	20fF
Supply V volt	8	5	3.3	2.5	0.6
Op. I mACV*f	1	0.1	. 01	1uA	10 nA
Speed nS	70	10	3	500 pS	100 pS
Power*Speed pJ	560	5	0.1	0.03	1 fJ
Wafer size inch	3.5	4	6	8	12
Density Gates	100	2000	20k	200k	1M

Fig. 8 below summarizes the CPI merits, design parameters for IV over past 5 decades. We depict the features of the SCMOS. SCL shall offer great enhancement, and is compatible to CMOS, thereby extending life cycles. As a result, SCL may serve a critical role in emerging microelectronics as industry seeks ideal high density, high speed, and low power SOC solutions.

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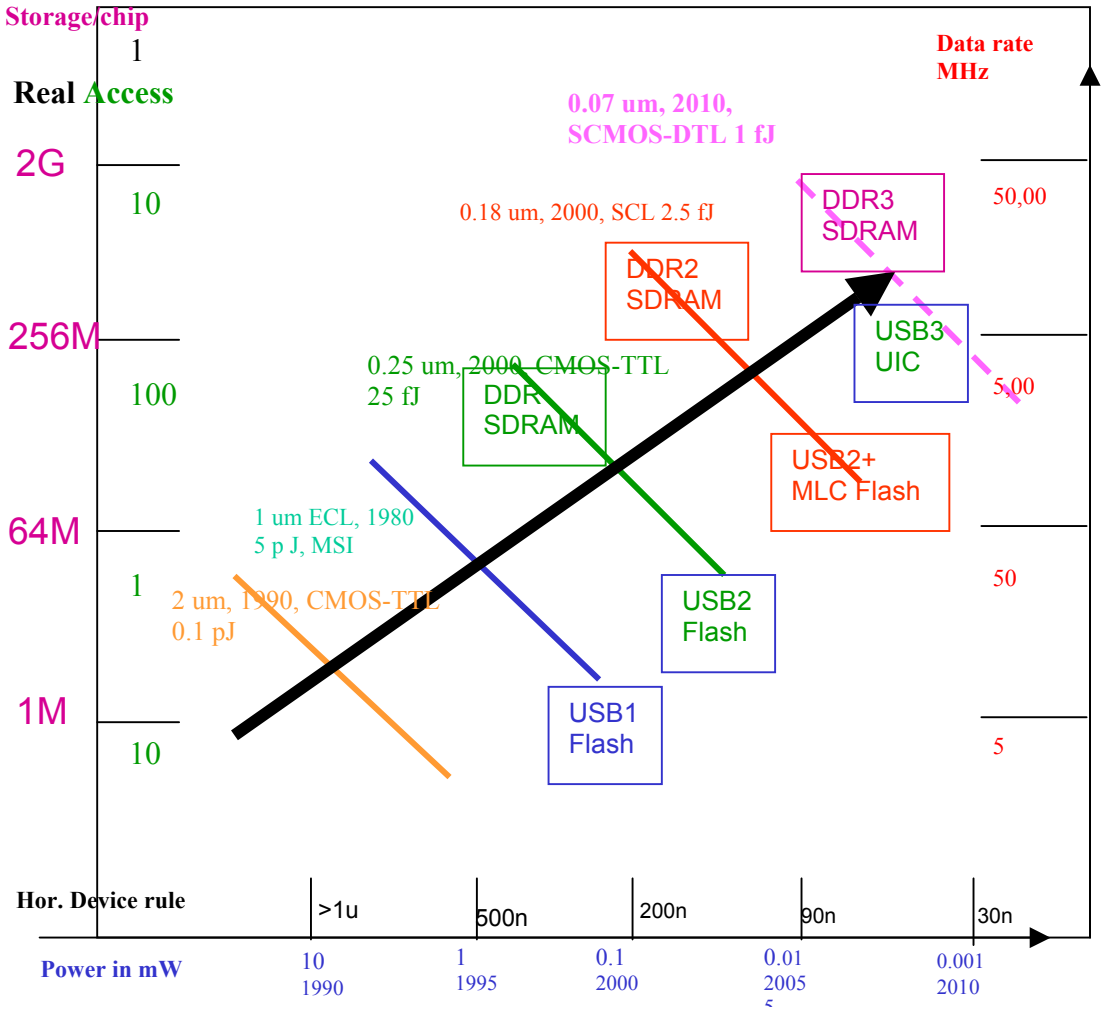

Fig. 8 The performance benchmark and trend chart of the logic and memory devices with microelectronics since 1990.

Fig. 9 illustrates a synopsis of SCMOS technology, product design concept, attributes, core competence, and system applications

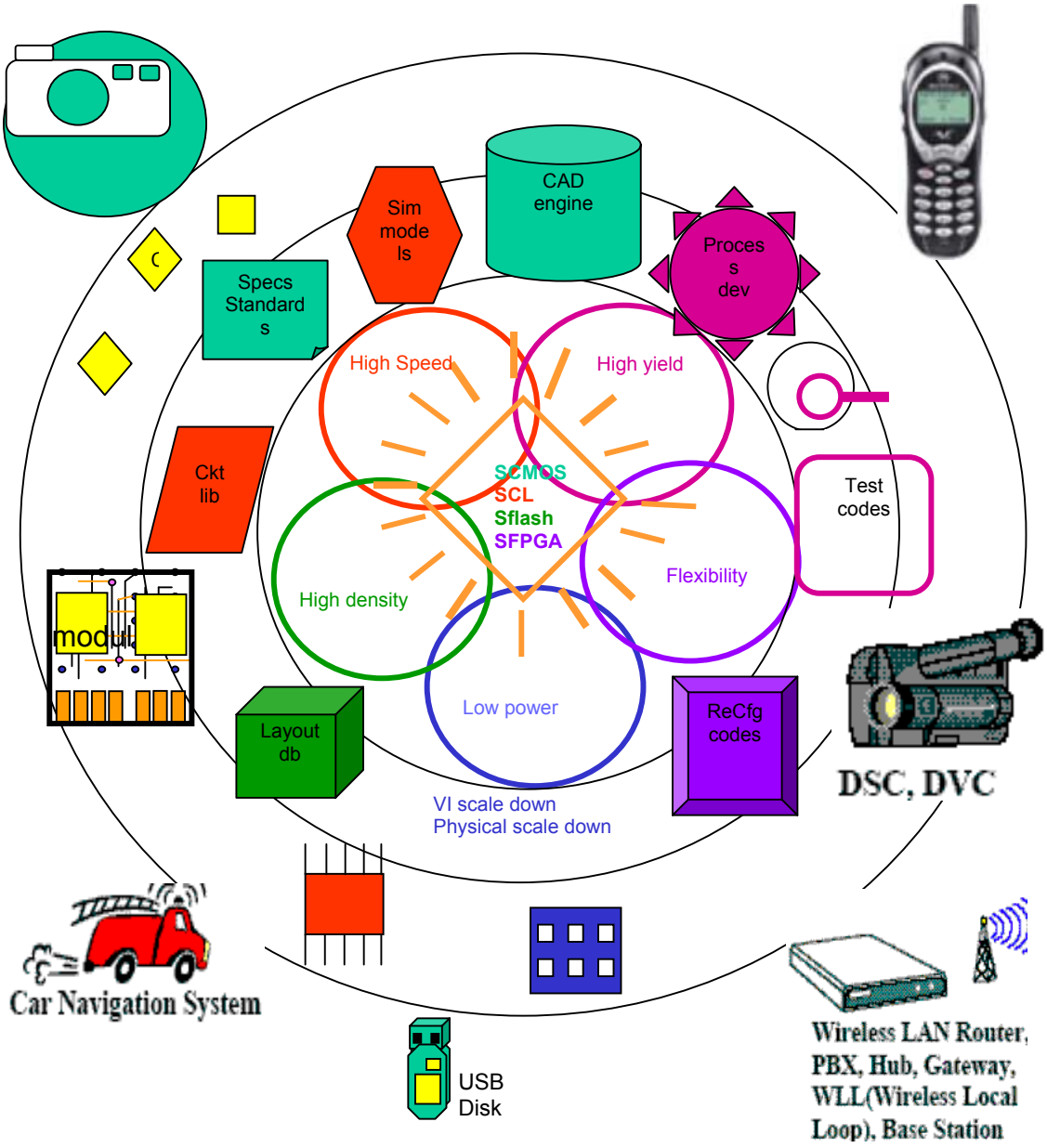

Fig. 9 A synopsis of SCMOS technology, attributes, core competence, and product applications.