The SCMOS Technology and Applications: an integrated circuit white paper

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Abstract

摘要

The SCMOS stands for Super CMOS. It is basically a new class of integrated devices equipped with low-level CMOS transistors, capacitors, resistors, and the newly invented low barrier Schottky Diodes (LBSBD) fabricated with isoplanary processes. However, significant differences are found in the high-level circuit configurations, device economics, dynamic circuit operations, less active nodes, total net counts, and low biasing supply voltages. Thus it opens a brand new class of microelectronics devices, all centered on the newly added low threshold Schottky barrier diode (LtSBD) with Co/Ti metal silicides. The work function of Co is 0.53 eV right in the middle of the Si electron and valence bands. So that we may form both P and N type SBDs with P or N type FETs in the extended N-/P- S/D pocket regions. Since the SBD can be made as attachments to the conventional CMOS or Flash transistors, the SCMOS device implementations may convert from existing CMOS and Flash macro files.

Circuit wise, besides the SCL circuitry [REF.1,2], we added the newly invented pulsed DTL (PDTL) configuration, which combines the old Diode Transistor Logic (DTL) and pass-transistor-logic (PTL), and forms highly economical, high performance circuits with lowest power consumptions. Small die size and simple nets favor better device yield, embedded field programmable units [REF. 3,4] may facilitate instant repair and service alterations. These features underline a strong cost-performance design platform, zero dead inventories, and support consumer oriented service operations. High speed and high capacity devices have wide applications in data acquisitions, especially benefiting to mobile SoC computing.

SCMOS 代表超级 CMOS。 它基本上是最新集成电路的一种收藏器件, 以基层单位之 CMOS 三极晶体管、电容器、电阻器、和新发明的二极管, 以单向开窗法过程制造。 然而，其重大区别在于高级电路结构、设备经济效益、动态电路操作，活跃网点少, 总网点少、和偏压电源低。 因而, 它开发了崭新一代之微电子产品, 围绕着最新发明的低障碍肖特基二极管(低障肖特基管). 此管(LtSBD)由钴/钛金属硅化物合成。 钴/钛的功能值是 0.53 eV 在硅正电子和负电子带的正当中。 因此我们可能在 S/D 地区延伸 N-/P-、寄生 P 或 N 型之 SBD 于 P 或 N 类型 FET 三极晶体管之中. 因此、SBD 可以被视作为常规 CMOS 或快閃晶体管的附件， SCMOS 设备实施也可从现有的 CMOS 和快閃晶体管宏指令集获得。

在电路上, 除肖特基-CMOS-逻辑[参考文 1,2] 之外, 我们加添了最新发明的脉冲 DTL (PDTL) 配置,它结合了传统的二极管逻辑(DTL)和通路晶体管逻辑(PTL)，形成了高度经济，高性能和最低功耗的电路。 小塊芯片和简单的网点数可期望更好的投产良率，嵌入式的现场可编程序功能单位 [参考文 3,4], 促进了芯片之立即修复和更改服务。 这些特点强调一个最佳的费用-功效设计平台，调零的呆货，并且支持消费者定向的服务操作。 高速和高容量设备在数据采集上有宽广应用，特别是有益于移动计算之单一芯片机(SoC)。

I. Introduction-The birth of the SCMOS Technology

I. 导言－SCMOS 技术的诞生

Ever since the introduction of the integrated circuits to the microelectronics industry, workers are seeking techniques to improve the functionality, performance, and capacity of the chips and their PCB assemblies. Trends were set to systematically driving for physical dimension and electrical signal shrinkage on one end, while considerable efforts are placed to enlarge wafer size, cleaning process and operations, enhance device yield and invented products and applications on the other. The results are astonishing to record the history that we created a booming economical business worthy trillion dollars global wide revenues each year. Further more, Information and its associated Technology (IT) penetrates every body’s life style and productivity when people are using the miniaturized devices and their computing power.

自集成电路的介绍到微电子产业，业者寻求技术改进芯片和他们的印刷版电路(PCB)的汇编功能、表现和容量。在实体和电信号方面, 趋向在缩小尺寸和降低振幅，而另一方面致力于提高设备出产量, 安置精密仪器, 扩大硅晶圆片大小、研制清洗的过程和化工操作，发明各种类型的产品和应用。结果是令人惊讶地不断刷新历史记录, 微电子产业已造就了兴旺的经济企业,在全球创造了每年值得上兆美元的收支。更进一步说，信息和它伴生的技术(IT), 当人们使用小型设备和他们的计算能力时,深入并革新了每个人的生活方式和生产力。

It was key that transistors were invented, which replaced vacuum tubes in the 1950s, integrated circuit arts were invented to house a number of circuit elements in a common wafer substrate in the early 1960s. During that era, main-frame computer using simple ICs was build to support space programs while establish commercial and scientific services in computing. The microelectronics industry walked through the early stages of IC with resistor-and-transistor coupled logic (RTL), diode-and-transistor coupled logic (DTL), and transistor-to-transistor coupled logic (TTL) as the basic circuit architectures for component advancement. By the 1980s, we settled in Emitter coupled logic (ECL) with the bipolar technology as the state of quote arts. IBM 360, 370, 380 were the bench marked computer systems each are selling for $M per million instructions per second (MIPS). Microcomputers was born from small potato like Intel in the late 1970s, and complementary metal on semiconductor (CMOS) was debuted in 1980s as new brand state of the art field-effect-transistor (FET) technology for its elegant device sizes and dc static operations both situated well for large scale integrations. The CMOS pushed several generations in personal computing with Intel’s Pentium machines and DEC’s server, it also benefited system houses like Sun Microsystems, and Microsoft, and Oracle for they excelled in system hardware and software applications.

具关键性的晶体管被发明了，在 50 年代它替换了真空管。在 20 世紀 60 年代初, 集成电路工艺被发明, 它安置一定数量之电路元件在一个共同的基体芯片上。 在那个时代里，集成电路制造的电脑主机已使用于太空计划，并广泛建立商业和科学的服务。微电子产业通过集成电路早期走过了以电阻器和三极晶体管相结合的逻辑(RTL)电路，二极管和三极晶体管相结合的逻辑(DTL) 电路, 和 transistor-to-transistor 三极晶体管自相结合的逻辑(TTL) 电路, 算是集成电路元器件的基本电路结构。 在 80 年代以前，人们相当满意于以射极耦合逻辑(ECL) 电路为基楚的双极性工艺技术。IBM 大卖 360， 370， 380 计算机系统。营业指标为每秒每百万次的指令運算(MIPS)售价为一百万美元。小土豆公司英特尔在 70 年代末期出现，并且以金硅(MOS)磁效晶体管(FET)技术制作微型计算机, 售价数百美元。在 80 年代里, 互补性金属半导体(CMOS)开张了。因为它具典雅的尺寸和静态操作俩大优点, 可作为新的大规模集成的品牌科技。 CMOS 在个人电脑领域推出了几个世代以英特尔的奔腾机器和迪吉多(康百克前身) 服务器，它也有益于系统公司如昇阳 Sun Microsystems, 微软 Microsoft，和甲古文 Oracle, 因为他们擅长在系统硬件和软件方面的应用。

Table I, IC chip design parameter trends

The trend of IC Chip design parameters
集成电路產品设计参数趋势

Tech. Rules/Pars	1970	1980	1990	2000	2010
Gox, Gate Oxide in Ang	4000	1000	200	70	30
Leff, Horizontal in uM	6	3	0.25	0.18	0.07
t, thin films in uM	1	0.5	0.3	0.2	0.1
Contact Size in uM	10	2	1.2	0.25	0.1
C, Load in pF	10	1	0.4	0.2	0.02
Vsupply	8.5	5.5	3.6	1.8	0.6
Vt in eV	0.8	1.2	0.9	0.5	0.4
I in mA	10	1	0.1	0.01	0.001
Speed in nS	70	10	3	0.5	0.1
Power*Speed in pJ	1000	500	10	0.1	0.001
Wafer size in INCH	3.5	4	6	8	12
Density gate counts	100	10,000	100,000	1,000,000	10,000,000
Density in MB	0.001	0.01	1	100	1,000

- **IC system application and driving forces**
- 集成电路系统应用和驱动力

Internet industry starts booming after 1990 when CMOS showed solid advantages over the Bipolar and the Bi-CMOS transitions. The IC demands had quantum jumps in processor speed and memory storages. During this period, PC and server industry prevails all computing business sectors. Big market boom proliferated IC HW and SW applications to enrich every body's life for information access and storage. Then the electrical erase able read only memory (EEPROM) or Flash device was introduced in the late 1990s, multilevel storage cell became reality after the turn of the century. The IC technology by now has been driven over 50 years. In the last decade, a strong real time data link and multimedia information processing demand created a big boom to IC products and applications. Wafer Fab facility advanced to 12 IN substrate, nanometer feature control, and 8 layers of on chip wiring is the new standard. Integration capacity of a memory chip measures at Giga-bits, and embedded processor speed running GHz.

在 1990 年以后, CMOS 以其坚实好处显示了优于双极和双极-CMOS 转型工艺时，互联网产业开始兴旺。 集成电路在处理器速度和记忆存贮俩方面市场须求有巨大突破。 在这期间，个人计算机和服务器产业战胜了所有计算的企业部门。 大市场景气激增, 集成电路硬件和软件应用丰富了每个人的生活忙于信息存取和存贮。 然后电子删除只读器(EEPROM)或快閃晶体管在 90 年代末期被介绍推广了，多重障存储元件(Multilevel storage cell) 在本世纪初以后成为了现实。 集成电路技术现在已被驱动了 50 年。在最近几年, 及时的数据链接和多媒体信息处理, 给集成电路产品和应用创造了更大的景气。流片厂的设施已推进了到了 12 寸晶圆片处理。新的标准是纳米级特点尺寸控制，并且在芯片上接线 8 个层数。单芯片之记忆存贮量已达数十亿比特, 嵌入式之处理器速度已达每秒数十亿赫次。

The most recent device innovation goes to the universal serial buffers, buffered processors, and wireless multi-path communications, so the personal computing devices, especially the mobile data processing units, for on-line data searching and acquisition are the more advanced. While the process state-of-the-arts is slowing down for it is reaching the minimum feature, the demand for the bandwidth of the data access chips/devices keeps growing. Any progress in maximizing capacity–performance-and power efficiency will meet strong resistances.

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The opportunity arrives for employing design innovations in IC. After the high capacity storage Flash devices, and multi-layer metal wiring (8) offered by the chemical-mechanical-polishing (CMP) processes, we offer the SCMOS and SCL as key SoC technology that would ease up circuit speed, process, system cooling, and battery life time problems of the CMOS bottle necks. We found that LtSBD and the newly invented Dynamic DTL configuration are new tramp cards in developing chip sets for low power computing.

最近之器件创新是统一型之串连缓冲器、带缓冲的处理器、和无线多重通道的通信器。因此个人电脑设备，特别是移动数据处理单位，为了网上数据搜寻和摘取, 将会是最先进的。 当前, 物理制程更新已到达了它的最后极限，而在片信息处理; 对数据存取芯片带宽的需求则有增无已。 任何增大容量, 强化功能, 和提高效率的举措都将遇见强度的抵抗。

在此, 吾人当有机会在集成电路中使用创新的设计理念。 在高容量存贮快閃设备, 和经由化工机械研磨制程(CMP)提供了多层金属接线之后，我们及时提供了 SCMOS 和 SCL 作为单芯片微机系统(SoC)之关键技术; 因其将能舒解电路速度,制程,系统冷却,和延长电池寿命等瓶颈问题。 我们发明了那低障肖特基管 LtSBD，并且最近添加了动态 DTL 电路配置,是开发低功耗计算,新芯片组合插卡的一张王牌。

The following sections introduce the emerging SCMOS solutions of circuit architecture, speed and power advantages, field programmable changes, and device manufacturing techniques to meet these challenges.

以下各部分介绍新兴的 SCMOS 电路架构、速度、和功耗好处、现场可编程序的操作、和接受这些挑战之器件投产技术。

2. Low Threshold Schottky Barrier Diode (LtSBD)-An Ideal I-V switches and for code storages.

2. 低障压肖特基二极管(LtSBD) -理想的 I-V 开关和代码存贮。

The Schottky contact barrier diode works on the theory of work function difference (WFD) between contact metal layer and Si bulk crystals. Depends on the selected reflective metal's work function-energies for its outer electrons to escape to vacuum space, the barrier height may be formed between the conduction/valence band of the semiconductor and the metal's conduction band. If Al or Pt was selected in the bipolar device era in the 1970s, when the author invented the High threshold SBD (HtSBD) in Bipolar ICs, the barrier height was then around 0.7 eV. The SBD threshold would clamp base-collector junction and suppresses deep saturation for shortening extra storage delays or triggers more severely the device latch-up actions burning up the chips from between power strips. If Cobalt or Titanium is used as contact barrier metal, then the work function difference is +- 500 mV respectively to either N- or P- terminal.

肖特基障碍二极管的操作理论是基于接触金属层和硅晶体之间有不同之功函数(WFD)。 取决于所选择的反射金属的功涵数-为该金属的外围电子能逃脱至真空之能量，障碍高度取决于金属和半导体的传导带或价位带之间。 如果在 70 双极器件时代，作者在双极 Ics 里,用鋁 Al 和 鉑 Pt 发明了高障压 SBD (HtSBD)，障碍高度大约 0.7 eV。 其时, SBD 可夹紧双极性三极管之基极和集极偏压,并且压制深饱和,缩短额外存贮延迟, 或消除了芯片上电源布线间,触发更加严重之死锁, 烧毁了芯片及器件组合。 如果使用钴或钛作为接触金属层金属，则到 N-或 P-终端之功函数差分别为+ - 500 mV。

We have postulated and verified that Co/Ti silicides SBD may make N-type or P-type SBD miniaturized diodes with Si surfaces, where each device occupies only single contact area in Si bulk. The barrier metal serves as Anode (to N- Si) or Cathode (to P- Si) terminal. The other terminal may be shared with those from souce or drain of the CMOS or the Flash transistors. Thus, SBDs can be economically attached to the large CMOS or Flash transistor's S/D bed, and hopefully have no adverse impact to transistor I_V characteristics.

我们假设和核实了钴/钛硅化物, 可在硅晶表面做成 N 型或 P 型的小型 SBD 二极管，每个元件只占占一个接触点的空间范围。 障碍金属担当阳极(到 N-硅晶 Si)或负极(到 P-硅晶 Si)终端。 另一个终端则可与 CMOS 或快閃晶体管的 S 或 D 极分享。 因此， SBDs 可以很经济地寄生于 CMOS 三极管或快閃晶体的 S/D 床中,并有希望无害于晶体管之电信 I_V 特征。

Simple logic gates and analog units can be formed with least real estates. Many macros such as the standard cell units may be easily derived functionally equivalent to existing CMOS gates but with simplified and reduced net in circuit topology, much smaller pocket sizes and total pocket counts, and operated with lower supply voltage and signal swings. The following drawings show the vertical and horizontal layout of CMOS and Flash transistor profiles where SBD are attached in the S/D pockets.

简单的逻辑门和类比单位可以花费最少之芯片地产。 许多宏指令例如标准逻辑单元, 能从现有等值功能的 CMOS 闸门, 轻易地改造而获得。但其在电路拓扑结构上被简化、减少了总网点计数,具更小的口袋大小，使用更低的电源电压和信号振幅。 以下图示显示了 CMOS 和快閃晶体管之垂直和水平的线路布局， SBD 是可附加在 S/D 口袋中的。

Process wise, the SBD can be attached to the FET transistors with minimum deviation only in low temperature contact metal treatments, and sub-region resistance implant as options to lower the cathode/anode resistances when performance requires. The very difference of the SBD barrier-metal-contact and the shared S/D contact lies in the N++/P++ contact diffusion treatment to the latter. Therefore, SBD contact region needs a block out mask during the S/D P++/N++ implants operation, so the barrier region has Barrier metal on N- or P- bed, a sub-implant region is served as an optional underpass to lower the diode body resistances in certain product embodiment.

制程方面， SBD 可以最小偏差共享磁效晶体管 FET 之一般处理,仅当功能需要时, 在抵抗金属处理阶段, 在肖特基二极管区域植入离子, 用以选择性的降低负极或阳极电阻。 SBD 障碍金属接触点与共有的 S/D 接触点的区别,在于后者有加 N++/P++扩散处理。 所以，SBD 管的障碍金属接触点区域, 在 S/D P++/N++植入操作期间，需要阻挡光罩。因此, 障碍金属接触点区域,有障碍金属, 在 N-或 P-硅晶床，并在某些产品实施中, 佈射地下过道以降低二极管管之电阻。

One can easily see that the SBD can be the by-products to both CMOS and Flash transistors when mixed functional units are embedded in a single chip. In this environment, the LtSBD is the smallest diode element for logic gates or switches, or memory bits for control codes or data storage. During the 2004 TSMC lab studies, the forward characteristics starts logarithmic linear at 1 uA for 0.1V drop, all the way to several mA. The reverse leakages are contained in a couple nA at 5V reverse biasing. Practically, it switches around the I-V origin steering uA currents, and operated at ~o.1 V biasing in the activated windows at extremely high speed and lowest power dissipation.

当单一芯片具嵌入式混杂的功能部件时, 你能容易地看到 SBD 可以做成是 CMOS 三极管和快閃晶体管的寄生物。在这个环境里， LtSBD 是最小的二极管电路元素,使用于逻辑门或开关,或者记忆单位做为控制码或数据之存储。 在 2004 年 TSMC 实验室研究期间，其前向电信特征,起始于 1 微安 uA, 0.1V 扁压, 以线性对数下落，一直到几个毫安 mA。 漏电量在 5V 反向偏压时,可在 2 奈安 nA 以内。 实际上，它在 I-V 源点附近以微安级 uA 之小电流,~o.1V 之偏压即可在脈冲窗口内启动开关功能,具极高速和最低的功耗数。

The SBD-CMOS logic (SCL) gates yield the smallest cell pitch sizes compared to any technology in the IC history. It has the least pitched wiring infrastructures (up to 8 planes) for interconnecting and driving with the best RC time constant possible for any circuit combinations, and it can be operated with single low value supply down to 0.6V.

SBD-CMOS 逻辑(SCL)门,已在集成电路历史上, 与所有技术比较, 产生了最小尺寸的开关细胞。 它将具有最少间距的接线基础设施(可堆积至 8 个平面) 。在互联和驱动所有电路组合时, 具最低的 RC 时间常数，并且它可使用单一低值电源--直落至 0.6V。

The SBD arrays can be made as ROM or one time programmable ROM by contact or via fuse/anti-fuses. Fine array core including decode and sense amp can be designed with 4F^2/bit core and 2F pitch for the peripheral circuitry realizing the best density for any IC arrays, and it performs at the best speed and lowest power consumptions. FPGA circuitry is also under development, which houses on-chip facilities for field changes or program alterations for repairs or customizations. No dead inventory and benefiting time-to-market for any engineering changes.

SBD 列阵可以作为 ROM, 或或通过熔丝或反熔丝手段, 作为一次性可编程序的 ROM。最精密的列阵核心包括解码器和感应放大器。设计精密度可以达到 4F^2/bit (F=最小物理尺寸) 之核心细胞, 和 2F 之间距, 实践了所有集成电路列阵的最佳周边电路;它执行最佳的速度和最低的功耗。 FPGA 电路也在发展中，在此芯片设施为了维修或客户定做, 提供在线更改或节目改变。 因应任何工程变化和市场需要提供及时服务,没有呆存货。

Many low power and high performance containing analog functional units for data accessing, PLL and charge pumps, RF and data converters, multi-level comparators, CRC streaming units, dsp units are under development. They will drastically change the picture from the current CMOS-TTL hardware.

许多低功耗和高性能类比功能部件包含数据处理，相位链锁 PLL 和电压灌注泵， 射频 RF 和数据转换器，多重电位比较器，循環重复检测 CRC,数码汇编单位等均在发展中。 他们从当前 CMOS-TTL 硬件方案中改变新型象。

Fig. 1, The SCMOS device profiles and the I-V characteristics of Schottky barrier diodes using various metals.

图. 1，SCMOS 设备外形和肖特基障碍二极管使用各种金属的电流-电压特征。

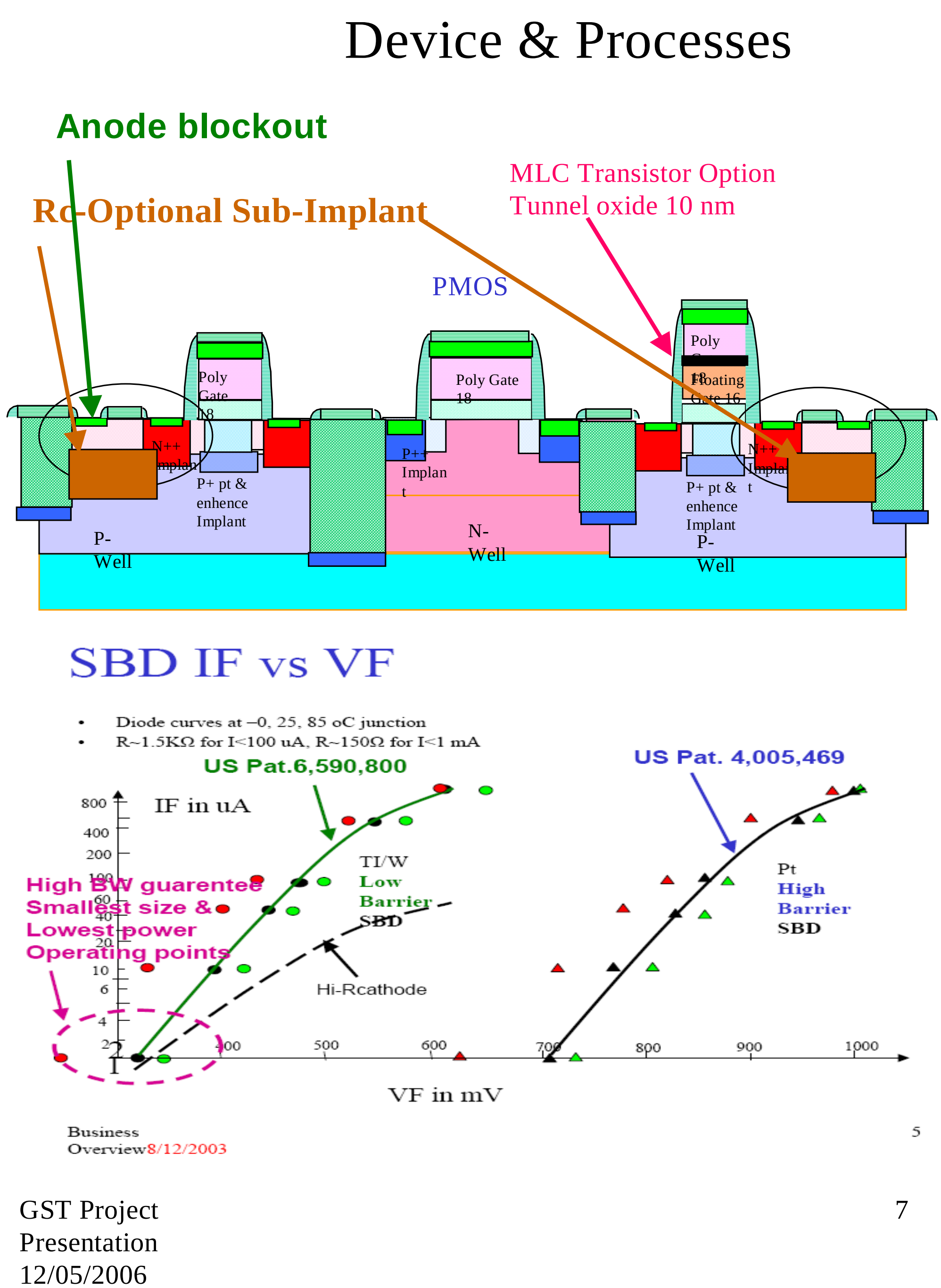
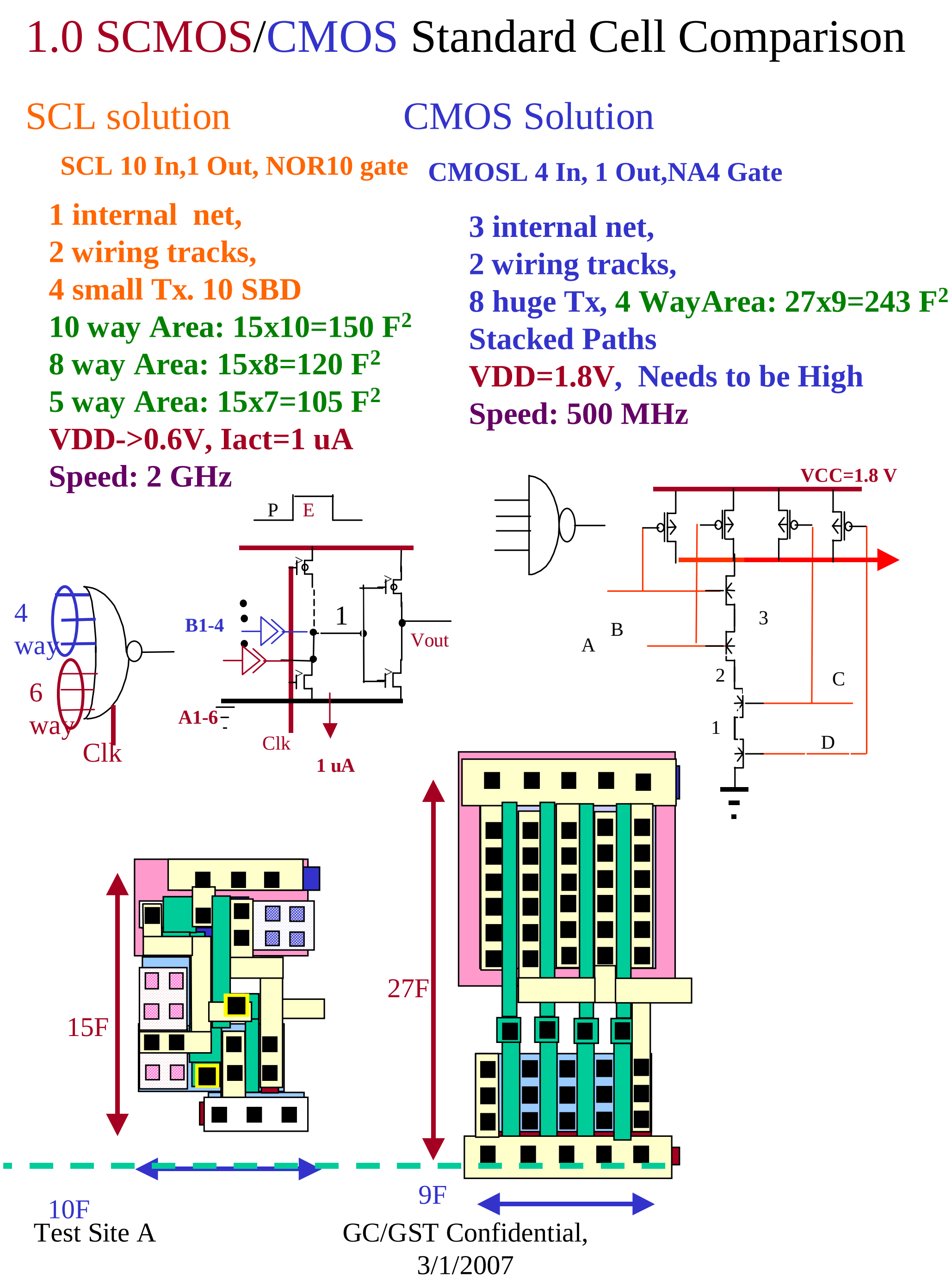


Fig. 2, The implementation comparison of SCMOS and CMOS logic gate.

图. 2, SCMOS 和 CMOS 逻辑闸门实施比较。



In the above SCMOS circuit schematics, block diagrams, vertical profile and horizontal layout of the SCMOS and CMOS logic gates, we see that the SCMOS gate has a DTL circuit configuration, and single internal node. It operates on a dynamic logic scheme. Logic values are realized only during the clocked window, otherwise they were blocked and may be ignored; or to serve different purpose such as for state indicator or biasing under a known (idle) state. However, the conventional CMOS gate is dc static, configured by TTL topology with more internal nodes and large device pockets. Therefore, it has a lot of inherent deficiency compared with SCMOS implementations.

在上述的 CMOS 和 SCMOS 电路概要、垂直结构图、和水平的逻辑门布局，我们看见 SCMOS 有一种 DTL 二极三极晶体管环扣逻辑闸之电路配置，并且仅有单一内部网点。 它以动态逻辑操作; 仅在脉冲的窗口期间，体现逻辑价值，否则他们将被阻拦并且应被忽略; 或使用于另外目的例如状态显示或为一个知道的状态(等待)作偏压。 然而, 常规的(CMOS TTL) 闸门是直流 dc 静态的，配置是基于三极晶体管自环扣逻辑(TTL)拓扑结构, 具多个内部网点和大的装置口袋。 因而，比起 SCMOS 它有很多先天缺点。

In SCMOS gate, the SBD occupies only single contact space, channels one signal path. The input device and channels are the SBDs, the output unit is the inverter. However, in the CMOS gate, signal applies to a pair of transistor gates as an input channel, each 4-way output drivers have legs of either 4 NMOS or 4 PMOS transistors. While the pockets are bulky, the associated RC time constants are huge; it drives immense loads of following gate pairs and wiring tracks. One can see the shortcomings of CMOS implementations, which inherently requires large Si area, higher power supply, huge signal swings, delay tolerance and variations.

在 SCMOS 闸门中，每个 SBD 仅占领单一接触点空间，提供一条信道渠道。 其 输入装置和渠道是 SBD 接触网点，输出装置是反向器。 然而，在 CMOS 闸门，每一信号道占用一对晶体管闸门作为输入通道，故 4 信道闸门有 4 支 NMOS 加 4 支 PMOS 晶体管的腿。 当此庞大的装置口袋被驱动时，伴生的 RC 时间常数是巨大的，它驱动下接之巨大负载;成对的门数和其接线轨道。 吾人当能看出 CMOS 实施之先天缺点:要求大 Si 地区面积、更大的功耗、巨大的信号振幅、很大的延迟常数和变异参数。

3. The SBD I_V characteristics and device model

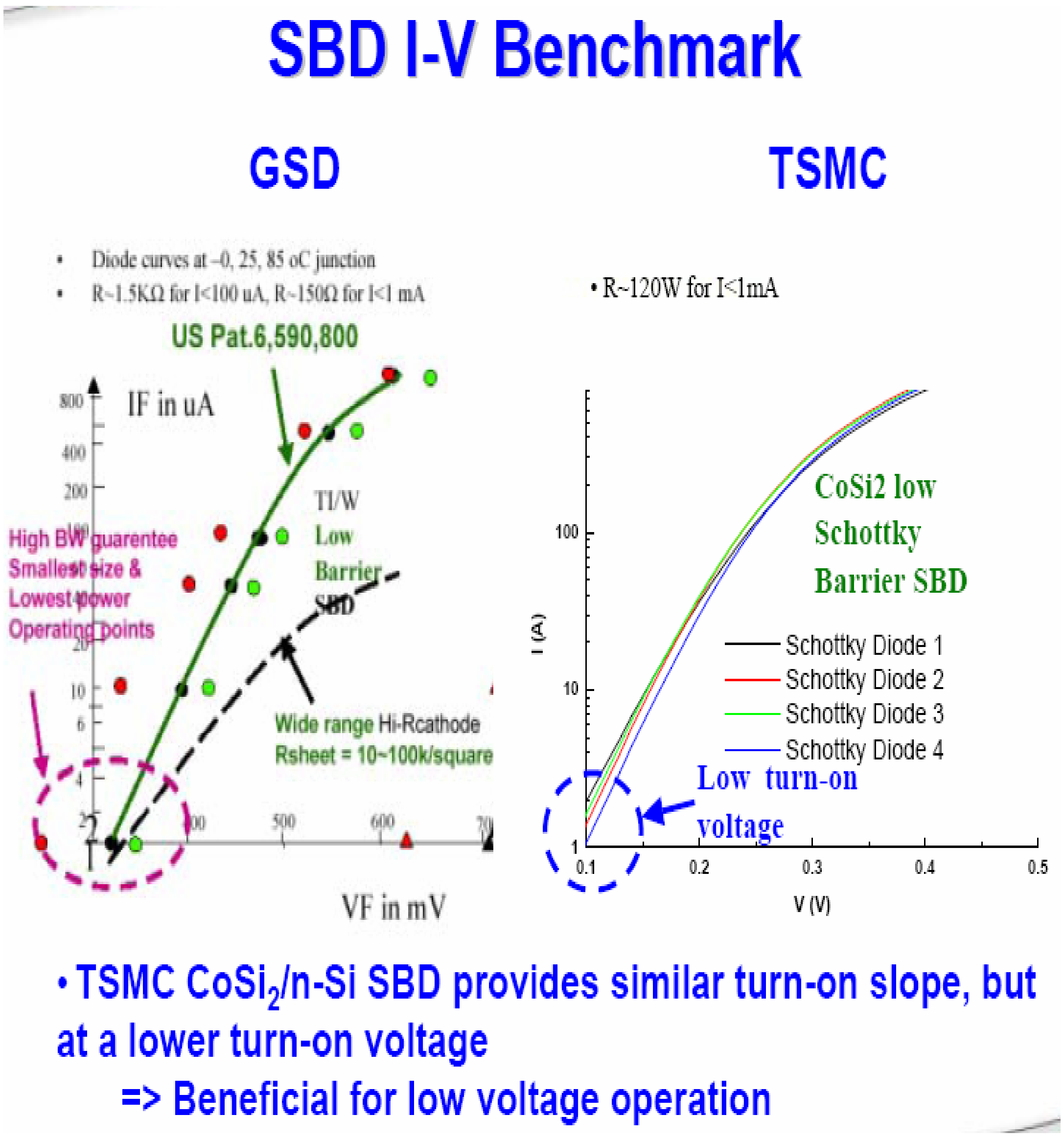
3. SBD 电流_电压特征和设备模型

The following theoretical model describes the thermo-ionic-emission current of the SBD device I-V characteristics adequately:

以下理论模型充分地描述 SBD 设备热离子放射电流的电流_电压特征：

Fig. 3, The Low Barrier SBD I_V curves from 4 device series families bench marked by TSMC

图 3, 由台积电 TSMC 提供, 从 4 系列低障碍 SBD 器件组所鉴定的 I_V 曲线图



Where J_T is the saturation current predicated on the barrier height and Kevin temperature. R is the Richardson constant, K is the Botzman constant. V is the terminal applied voltage, and the A is the barrier

这里, JT 是在障碍高度和凯文温度断言的饱和电流。 R 是 Richardson 常数， K 是 Botzman 常数。 v 是终端应用的电压，并且 A 是障碍

J_T=R(T+273)^2*EXP(-q*Vb/(K*(T+273))) (1)

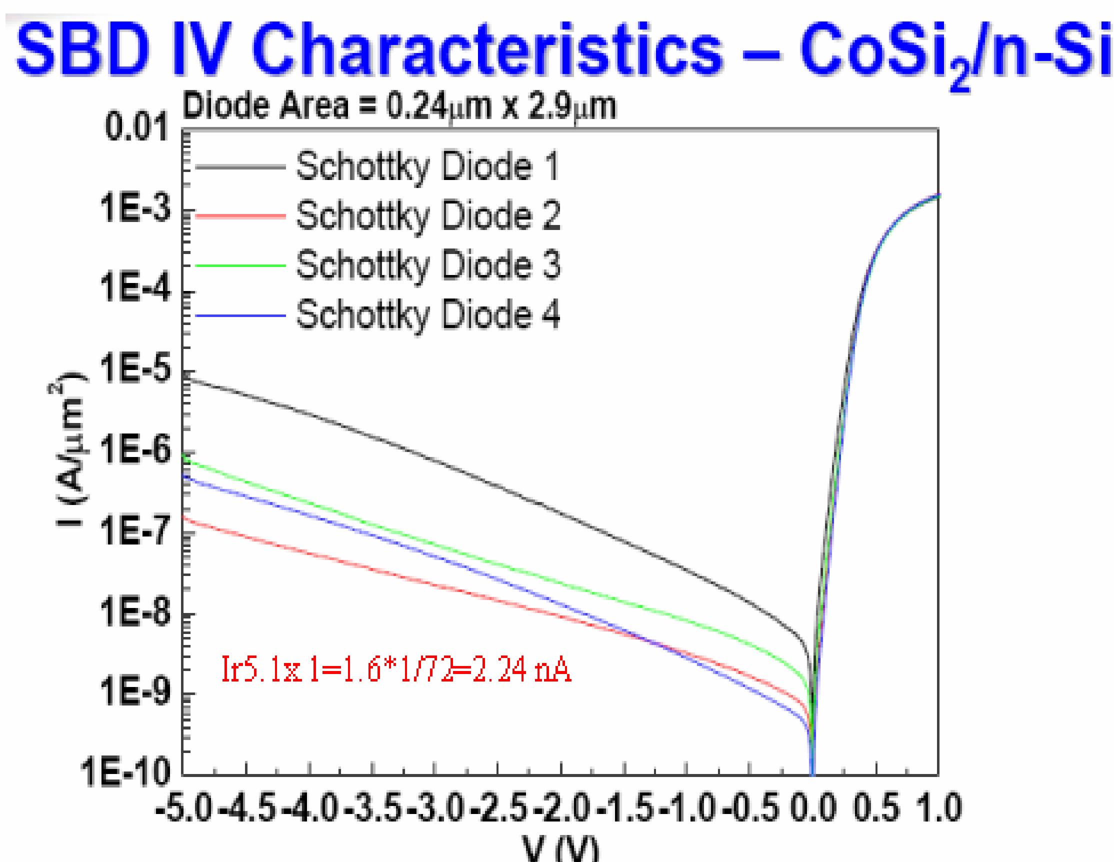
I_T=A*J*(EXP(qVF/(K*(T+273)))) (2)

contact area. The model has been verified by the data points measured in TSMC's lab at room temperature as show below,

联系范围。 模型由在 TSMC 的实验室测量的数据点核实了在室温作为展示如下

Fig. 4. The forward and reverse data points of LSBD devices measured by TSMC Data points exhibited acceptable diode curves of a miniaturized diode by TSMC lab. Good test wafer data points below extracted to 0.1xo.1 um diode with 1 uA at 0.1 V forward, and 2 nA at 5V reverse leakage.

图**. 4. TSMC** 之 **LtSBD** 前向和反向数据点。**TSMC** 实验室于 **2004** 年**,**生产并测定了几组小型化的二极管的 **I_V** 曲线如下。好的测试晶圆数据点**,**提取了对 **0.1xo.1 um** 二极管之前向起动从 **1 uA, 0.1 V** 反向漏电约 **2 nA,-5V**。



	Current@V=1V	Current@V=-5V
Schottky Diode 1	1.44 mA/µm^2	9.81E-06
Schottky Diode 2	1.56 mA/µm^2	1.61E-07
Schottky Diode 3	1.50 mA/µm^2	9.23E-07
Schottky Diode 4	1.54 mA/µm^2	5.21E-07

4. Wide device applications and macros design examples

4. 宽广的设备应用和宏指令设计泛例

The low barrier threshold (0.1V) of the LtSBD made it an ideal choice to clamp modern CMOS transistors, which has typical Vtn/Vtp value around 0.5V. The Vt difference between SBD and FET made it suitable to do several things efficiently.

LtSBD 之低障碍门限(Vtd=0.1V)使它成为一个理想的选择;夹紧现代 CMOS 三极晶体管，其典型的 Vtn/Vtp 价值约在 0.5V 附近。 因 SBD 和 FET 的 Vt 区别,使它能高效率地做几件事。

1). Serve ESD protection for input gates.
1). 为输入闸门提供 ESD 保护。
2). Suppress transistor I-Vs, prevent well latch-ups.
2). 压制晶体管的 I-V 功能，防止器件井袋间死锁。
3). Detect Audio/Video signals using diode-resistor rectifiers or decoders.
3). 使用二极管电阻器之整流或译码组合,解出音频或视频信号
4). Build on-chip voltage ladder and charge pumps using diode-capacitor clipping legs.
4). 建造在片增压器, 使用二极管电容器,修造电压梯子和电荷灌注泵。
5). Do logic and/or or NAND/NOR trees
5). 做逻辑与/或闸门 and/or 和与非/或非闸门 NAND/NOR
6). Do signal level shifting in I/O blocks.
6).在输入/输出块作成信号振幅转移。
7). Build, the low cost and high speed, densest storage arrays
   The theoretical limitation is 4F^2/bit, where F is the minimum feature size-say 0.18 um using the logic processes. Core utilitization factor is the highest for all Ics.
7). 修造便宜，高速，和最密集的存贮列阵
   理论极限是 4F^2/bit， F 是最小的特点尺寸, 如使用逻辑 180 纳米加工,大小在 0.18 um 。
   核心的有效使用因素 Utilitization Factor 为所有集成电路中之最高。
8). Perform Flash device based binary, ternary, and quaternary computing, multiple-bit analog-to-digital (ATD)/digital-to-analog (DTA) comparators and converters [REF. 3,4].
8). 进行基于快閃设备之二进制，三进制和四进制计算，多位类比到数码 (ATD) /数码到类比(DTA) 比较器和交换器[参考文 3,4] 。

Most importantly, we keep on finding useful traits of the LtSBD for it exhibits the finest switching and analog properties with simplicity and efficiency built-in.

最重要的是我们继续发现 LtSBD 有用的特征,因为它内涵了精简高效,陈现最美好的开关和类比功能。

Circuit/layout wise, the LSBD is a cute little piece circuit element-the smallest entity of any integrated components with common anode or common cathode bed sharing with the FET transistor source/drain nodes. Because the newly defined Schottky CMOS logic (SCL) is composed of a tiny dynamically operated current source with branching diode trees, it greatly simplified the TTL logic circuitry with greatly reduced on-chip active net counts (to 1/3 rd), transistor counts, and parasitic pocket counts.

在电路或布局方面， LtSBD 是所有集成电路组合中,逗人喜爱的最小的电路元素,这最小的个体与 FET 晶体管分享源共同的源或流极或共同的阴/阳极床。 由于最近被定义的肖特基 CMOS 逻辑(SCL) 是由一个微小的动态电源与分支的二极管树组成，它很大地简化了传统 TTL 逻辑电路;减少了在芯片活跃网点净计数(约至 1/3)，三极晶体管计数和寄生口袋计数。

The result is that logic switching is much cleaner, and much faster. Power-Speed trade off improved with gigantic TTL nets disappeared; the replaced DTL nets are both reduced in active net counts, and lowered associated RC time constants (i.e., inverters driving smaller pockets and wiring pitches comparing with TTL nets).

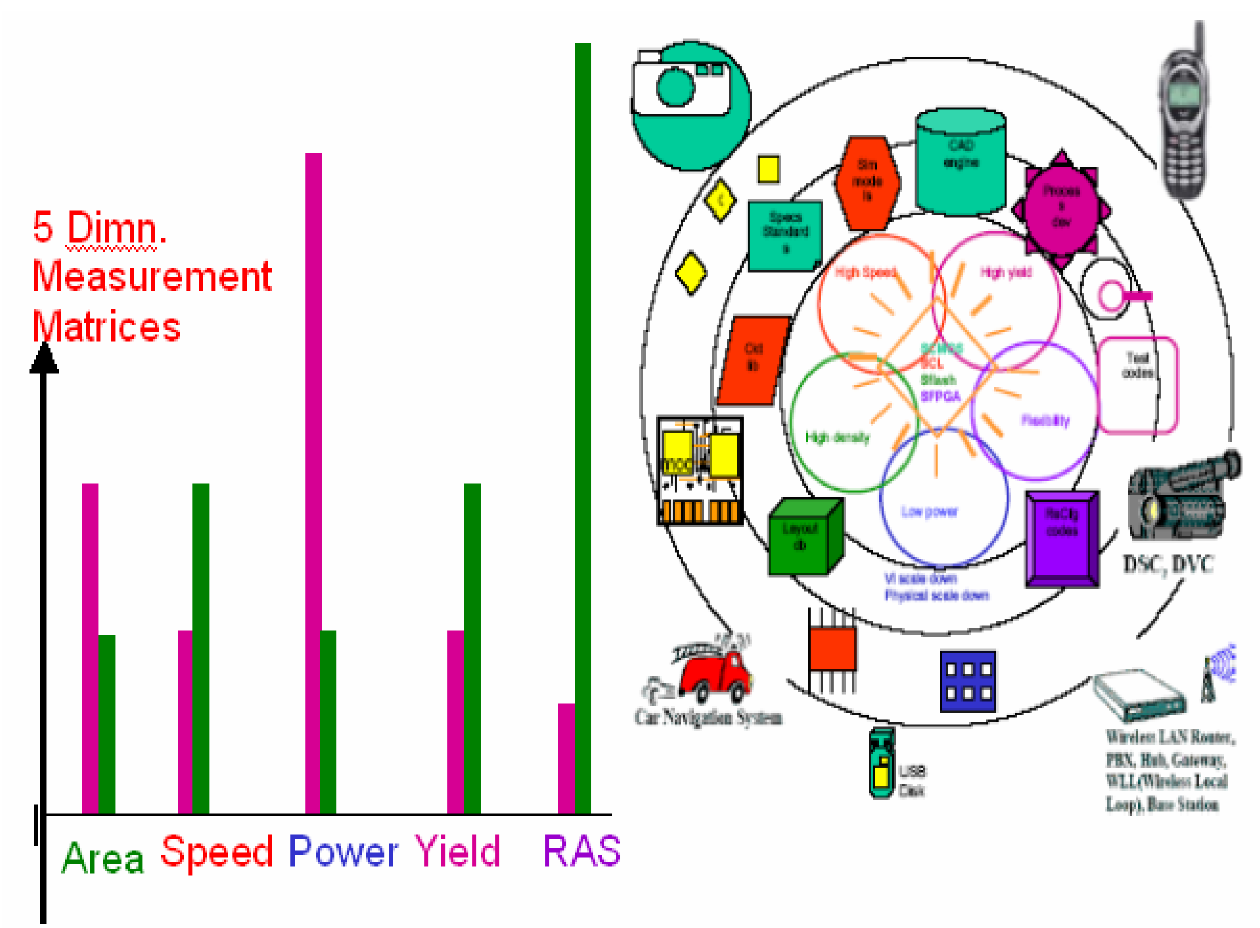
结果逻辑开关是更加干净和快速。 功耗-速度之交易更有进展,硕大的 TTL 网消失了; 被替换的 DTL 网具有减少的活跃网点,伴生的 RC 时间常数亦下降(即驱动更小的口袋和架线)。

Power supply, required by SCL, may be dropped to just above the FET threshold Vt (say ~0.6V), now that we get simple inverters driving DTL stages everywhere. In general, power consumption for any net is proportional to the square of the supply voltage and ac currents. If Vsupply lowers to ½, power reduction shall reduce to ¼. The SCL has significantly smaller layout areas; parasitic capacitances with wirings and pockets, hence the power advantage is more than 4X. This would not be possible to achieve with conventional CMOS TTL circuitry since it has inherently topological and structural disadvantages.

即然我们能到处以 DTL 驱动 DTL, 则 SCL 可使用单一的低值电源;仅需高过磁效晶体管 FET 的门限 Vt (约~0.5V)。 一般来说，功耗为所有网上与电源电压和其电流的乘积或电压平方成正比。 如果 Vsupply 降下½，功耗将减少到¼。 此外,SCL 有显着更小的布局区域; 接线和口袋寄生电容特小，因此功耗好处比 4X 是更多。常规之 CMOS TTL 电路, 因为它固有拓扑学和结构缺点，是不可能达到的。

Fig.5, SCMOS device design kernel, and cost-performance matrices

图形.5, SCMOS 设备，设计核心，和费用-功能标签



- **Implementation of functional macros**
- 功能宏指令集的实施

Basic Macro set was defined to yield useful embedded physical implementations starting with standard cells, pass-transistor logics, latch and D-type flip flops, SBD, Flash, and RAM arrays, IO pad ring units, and clock drivers, PLL units.

基本的宏指令集,可开始以嵌入式之物理设施、通过晶体管逻辑、门闩和 D 类型触发器， SBD、快閃和 RAM 列阵， IO 接线版单位, 和时钟驱动器，相位链锁 PLL 单位,产生有用的标准单元。

An Analog-Logic-Memory (ALM) product library for the mixed signal macro set has been defined below,

以下是类比,逻辑,记忆(ALM)产品库的混合信号宏指令集之定义，

Table II, Schottky Circuit Constructs for the Examplary SCL ALM Units
表 II，SCL 电路, ALM 单位之示范修建
1.SCL, PTL, SAnalog Basic units
1.基本类比, 逻辑单元
2.Sconverters
2.SCL 类比, 逻辑转换器
3.Mask SROM
3.SCL 光罩编程的点阵记忆体 ROM
4.SSRAM
4.SCL 静忒记忆体
5.DRAM-SPSRAM
5.SCL 动忒记忆体
6.Sflash
6. SCL 快閃电路
7.SFPGA
7. SCL 可编程的快閃列阵
8.SPLL/DLL
8. SCL 相位链锁环/延迟线链锁环
9.Image Sensor or Sigma Delta Converter
9. SCL 音影数码转换器
10.MMU/Cache16 or Wallace Tree 16
10. SCL 16 位元记忆体控制,高速缓冲, 乘法器

Figure 6 below shows SCMOS based IO buffer and the 4T Schmitt trigger circuit schematics.

图 **6,** 展示了 SCMOS 之 IO 缓冲和 **4(三极)管触发器** 4T Schmitt Trigger 电路。

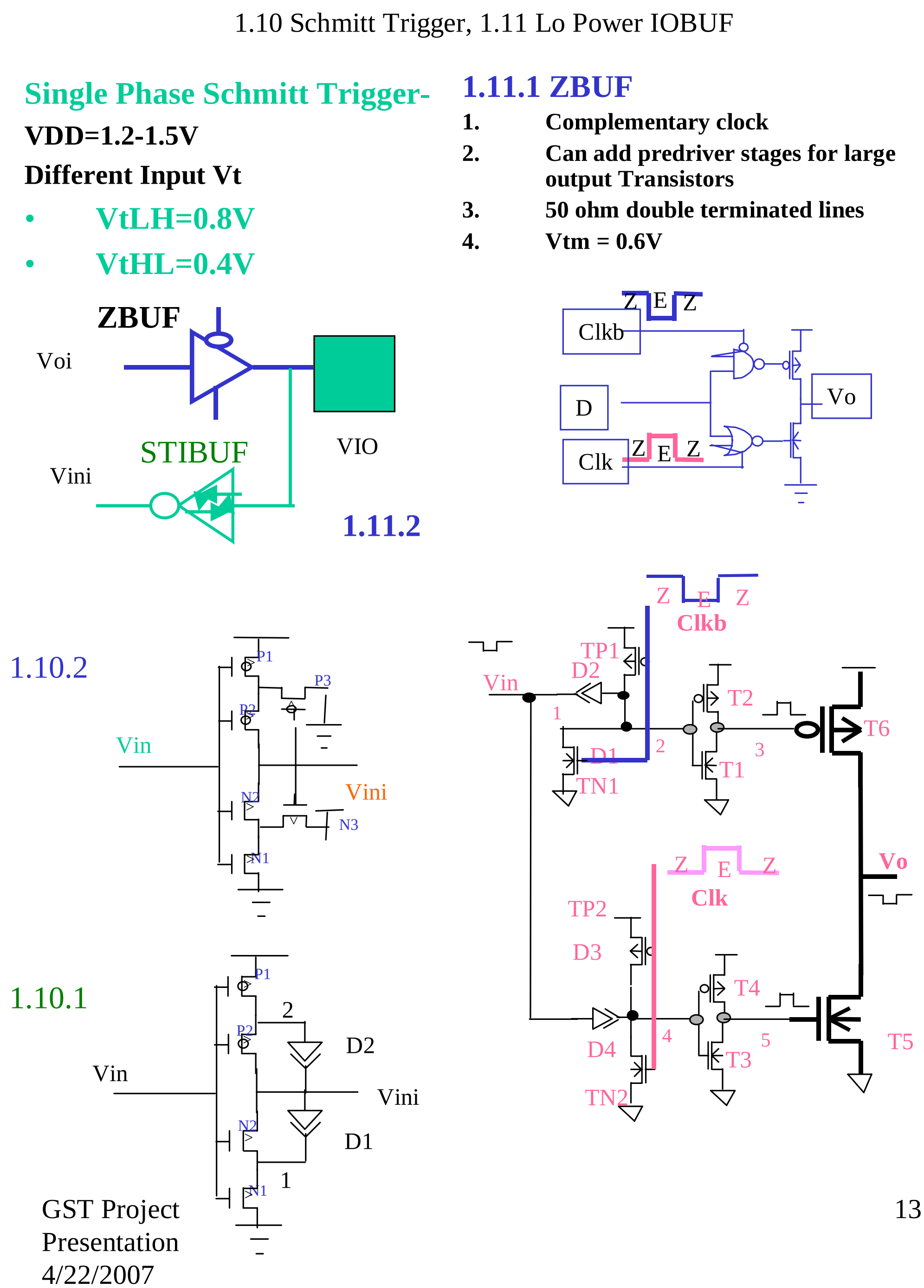


Fig.7 below shows Schematics of a nibble bank of of transceivers.

图 7. 在下展示 **SCMOS** 脉冲收发器半位元组(4bit) 之线路图。

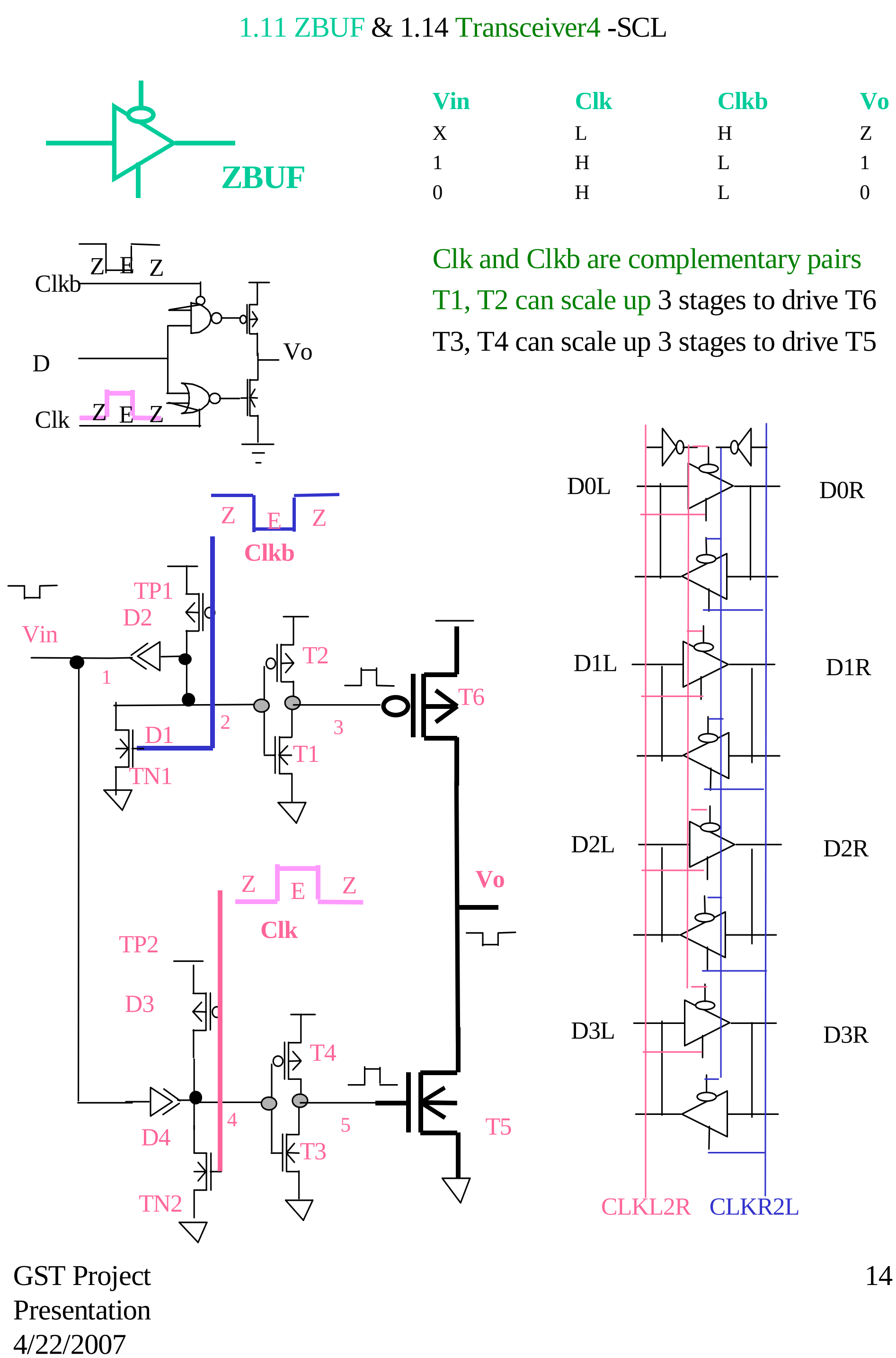
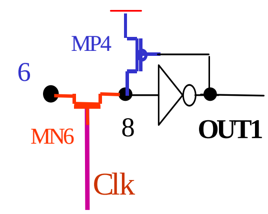


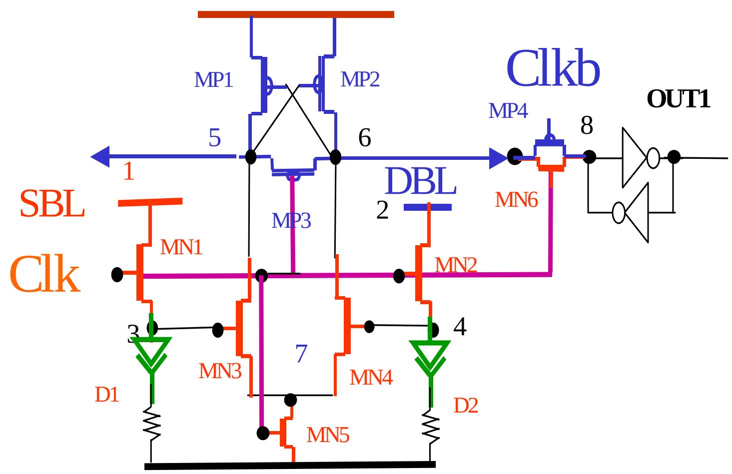
Fig. 8 below shows the Sense Amp with latch for the array core.
图 8 下面显示列阵核心之 **SCMOS 信号感应放大器与门闩**

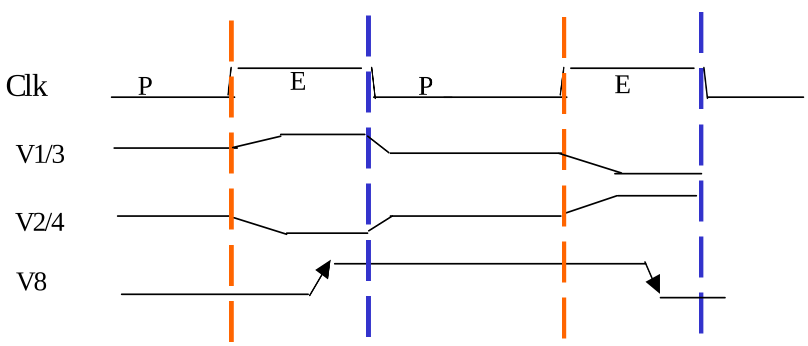
2.1 IOBUF/Sense Latch

Dual Phase Dynamic Sense Amp

- Hi embedded resistors with D1, D2
- Diff Inputs may be at V3, V4
- Diff Inputs may be at V1, V2
- 4T Latch Output option







Sense Amp Operation

Precharge: D1, D2 clamp MN3,4,5 OFF.

Evaluate: V3,4 pulsed on>>MN3,4,5 turned on>>MP1,2,3 Latching>>Output Latch reset

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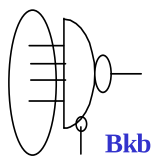
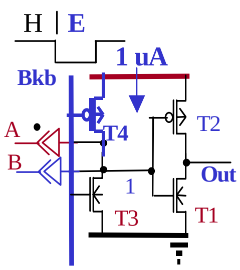
Fig.9 below shows the layout of **SCMOS standard cell NAND and NOR** macros.
图 9.下面显示标准单元与非和或非宏指令布局。

1a. SCMOS Pulsed Logic Units

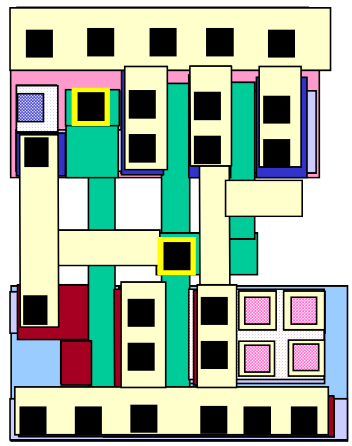
- 1.1.0 PNA1
- 1.1.1 PNO1
- 1.1.2 PNA2
- 1.1.3 PNA4
- 1.1.3 PNA6
- 1.1.4. PNA10
- 1.2.1 NA2
- 1.2.2 NA4
- 1.3.1 PNO3
- 1.3.2 PNO4
- 1.3.3 PNO5
- 1.3.4 PNO8
- 1.4.1 NO2
- 1.4.2 NO4
- 1.5.1 ROSC51SNA1
- 1.5.2 ROSC51N
- 1.5.3 ROSC51SNA2
- 1.5.4 ROSC51NA2
- 1.5.5 ROSC51SNA4
- 1.5.6 ROSC51NA4
- 1.5.7 ROSC51SNA6
- 1.5.8 ROSC51NA10
- 1.6.1 ROSC51SNO1
- 1.6.2 ROSC51IN
- 1.6.3 ROSC51SNO2
- 1.6.4 ROSC51NO2
- 1.6.5 ROSC51SNO4
- 1.6.6 ROSC51NO4
- 1.6.7 ROSC51SNO6
- 1.6.8 ROSC51NO10

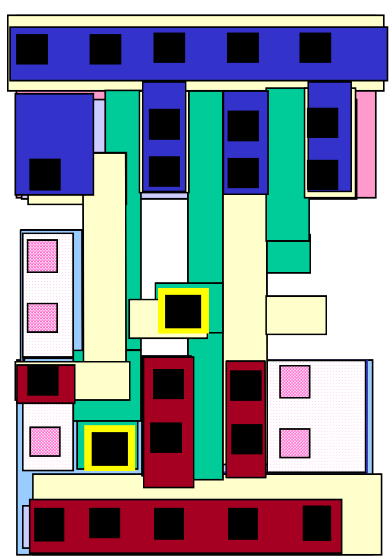


In A B	Bkb	Out PNA
- -	H	H
0 0	L	1
0 1	L	1
1 0	L	1
1 1	L	0

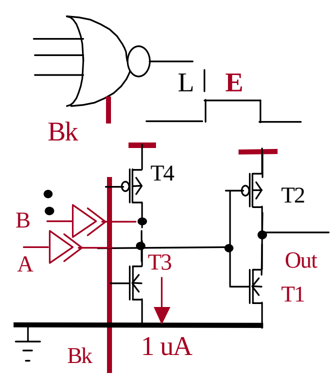


1.1.3 Hi Speed PNA5





1.3.3 Hi Speed
PNO3



In A B	Bk	Out PNO2
- -	L	L
0 0	H	1
0 1	H	0
1 0	H	0
1 1	H	0

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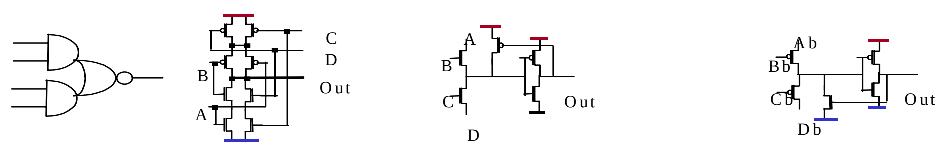
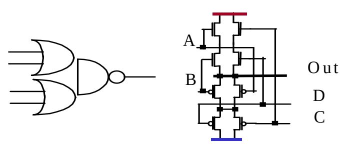
The P and NMOS inverter are both 4F wide (Tall). There are 2 wiring tracks in the center region. Logic diodes can be either N or P types, and the clock transistors can be the narrow width transistor for the critical current source limiter, or the short channel transistor for the non-critical leg. The wiring tracks are stacked in vertical planes (M1-6 layers), CMP metal rules are border less hence units are compact and high speed.
P 和 NMOS 反向器都是 4F（高）。在中心区域有 2 条架线的轨道。 逻辑二极管可以是 N 或 P 类型，并且时钟晶体管，如为节制重要来电流，则可用狭窄的晶体管. 如为不重要的腿, 则可用短渠道晶体管。 接线轨道在垂直平面(M1-6 被堆积层数)，跨層接点，使用 CMP 金属无边界规则以确保紧凑和高速。

Fig.10, and Fig.11 below show another class of diode tree based pass transistor logic (DPTL), which is highly area-speed-power efficient.
图 10 和图 11。下面显示另一类基于二极管树与通道晶体管逻辑(DPTL)，具高度之区域速度功耗效率。

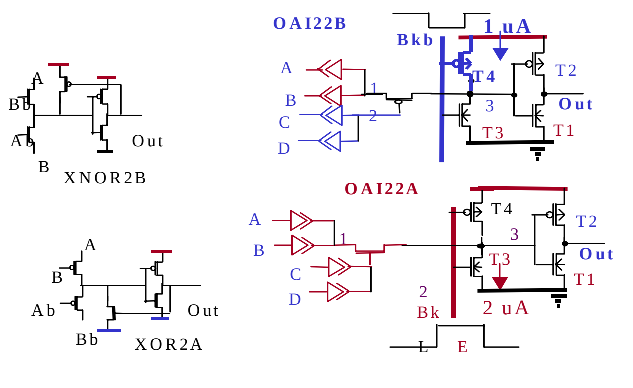
1.7 Pulsed Diode Pass Tx Logic (PDPTL), AOI & OAI

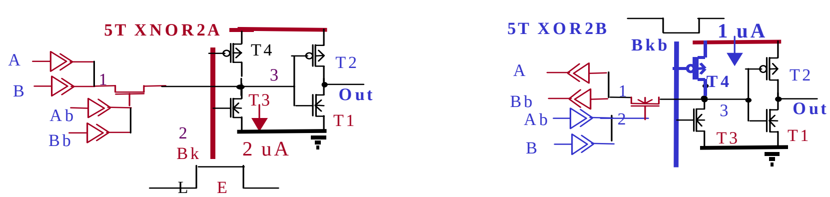




Truth Table of SCMOS gate AOI22B					
Bkb	A	B	C	D	
H	Don't Care	Don't Care	Don't Care	Don't Care	
L	1	1	Don't Care	Don't Care	
L	Don't Care	Don't Care	1	1	
L	0	Don't Care	Don't Care	Don't Care	
L	Don't Care	0	Don't Care	Don't Care	
L	Don't Care	Don't Care	0	Don't Care	
L	Don't Care	Don't Care	Don't Care	0	

1.7.1 8T AOI22
1.7.2 8T OAI22
1.7.3 5T AOI22B
1.7.4 5T AOI22A
1.7.5 5T OAI22B
1.7.6 5T OAI22A
1.8.1 5T XNOR2B
1.8.2 5T XOR2A
1.8.3 5T XNOR2A
1.8.4 5T XOR2B





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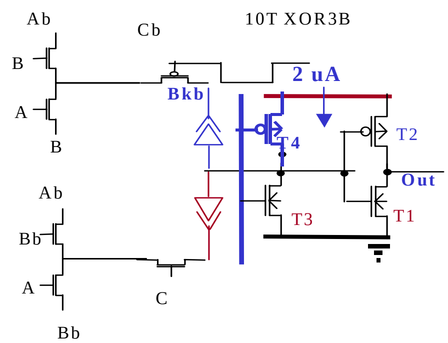
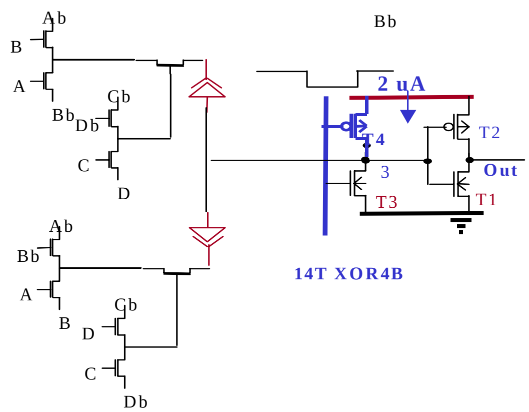
PDPTL, XOR Gates-continue



- 1.8.5 10T XOR3B
- 1.8.6 14T XOR4B
- 1.8.7 XOR5
- 1.8.8 XOR6
- 1.8.9 XOR7
- 1.8.10 XOR8



Comparison of conventional CMOS and DPTL Implementations								
	CMOS-TTL				SCMOS-DPTL(estimated)			
Functions		area	speed	mWatts		area	speed	mWatts
AOI22		10	1	10		6	5	1
XOR2		10	1	10		6	5	1
XNOR3		30	0.3	30		12	2	2
XOR4		40	0.2	40		15	1	3

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Here, the diode tree may perform logic operations with the pass transistor S/D and the Gate node to implement complex logic functions. The result is reduced transistor counts and area saving, plus speed-power improvement. Classically, the CMOS-TTL implementation needs 8 3-terminal transistors for the AOI22 or XOR2, the PDPTL reduces them to 5T.

这里，二极管树与通道晶体管之 S/D 和门进行逻辑操作完成复杂逻辑功能。 结果是减少晶体管计数和面积，加上速度功耗改善。 传统的 CMOS-TTL AOI22 或 Since area is primarily predicated on the isolated transistors, the attachment of diode tree to 3 XOR2 实施需要 8 支三极晶体管， 但 PDPTL 使他们降低到 5 支三极晶体管。

Since the compounded diode- transistors logic maximizes the overall area efficiency, hence the SCMOS approach greatly enhances the area-speed-power advantages of the overall implementations, far better than what was achievable by the conventional CMOS-TTL constructs.

因为大量混合二极与三极晶体管能强化面积,速度,和功耗的整体设备效率，因此可达成远远超越常规 CMOS-TTL 的实施。

- **The Latch implementations with the SCMOS**
- SCMOS 门闩的实施
-

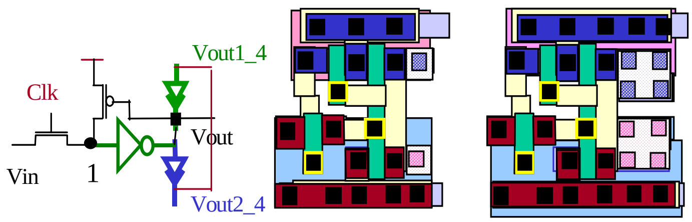
Figures 12, 13, 14 below shows the implementation of the latches, DFF, shift registers and counters. The SCMOS implementations support both rail to rail signal level for CMOS and also for SCMOS signal interfaces with diode offset.
以下图 12， 13， 14 显示门闩， DFF、移位寄存器和计数的实施。 SCMOS 实施支持 CMOS 所需的全幅振荡信号,并且也提供有二极管偏压差距的 SCMOS 信号接口。

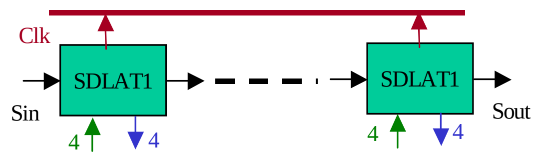
Fig. 12, SCMOS Larch

1.10 SDlatch, 1.11 SBD Muxes

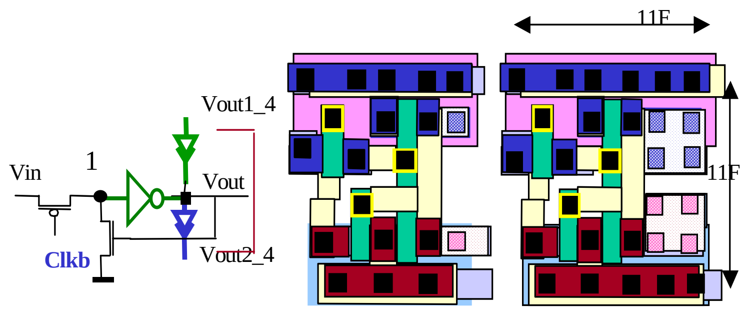
Multivalued Flexible Latches

- All Min Dimn Tx
- Add SBD for 4Set/4Reset buses
- SBD stripe for Mux8
- Universal SBDout-Vtd offset from VCC or GND.



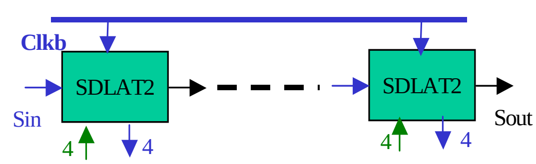


- CMOS level Vout
- SCL level Vout1
- SCL level Vout2



- 2.1 4T SDlat1
- 2.1 4T SDlat1_4
- 3.1 4T SDMUX8

- 2.2.4T SDlat1
- 2.2.4T SDlat1_4
- 3.2 4T SDMUX8



Comparison of CMOS and SCMOS storage logic cells							
	Classic CMOS		SCMOS				
		Signal		Signal			
Dlatch		CMOS		CMOS&SCMOS			
DFF		CMOS		CMOS&SCMOS			

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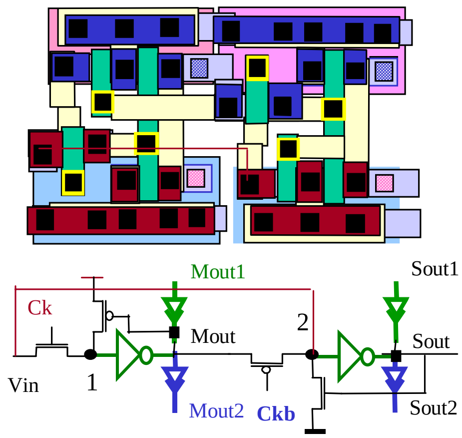
Fig. 13, SCMOS DFF

1.12 8T SDFF

1.12.1 Ckb activated

8T SDFF1

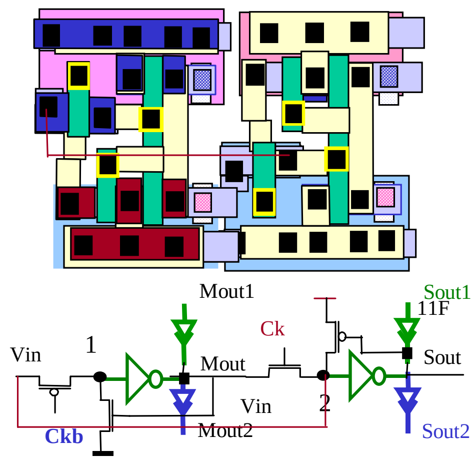
- DC static level clock triggered.
- 3 level signal out
- Master side **Reset**
- Slave side **Set**
- Master or Slave side Diode Muxes for Scan Master (Not Shown)
- Pass Tx Scan path option at Slave latch.
- Universal SBDout-Vtd offset from VCC or GND.



1.12.2 Ck activated

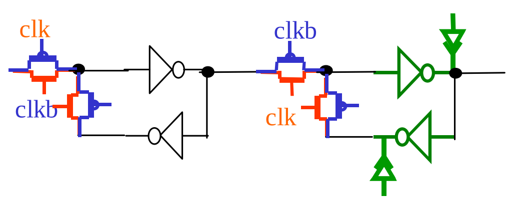
8T SDFF2

- DC static level clock triggered.
- 3 level signal out
- Master side **Set**
- Slave side **Reset**
- Master or Slave side Diode Muxes for Scan Master (Not Shown)
- Pass Tx Scan path option at Slave latch
- Universal SBDout-Vtd offset from VCC or GND.



1.12.3 CMOS prior Arts

- 16 T DFF
- 24T Set/Reset DFF



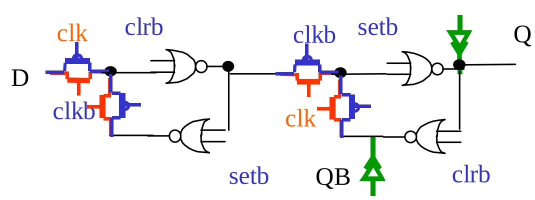


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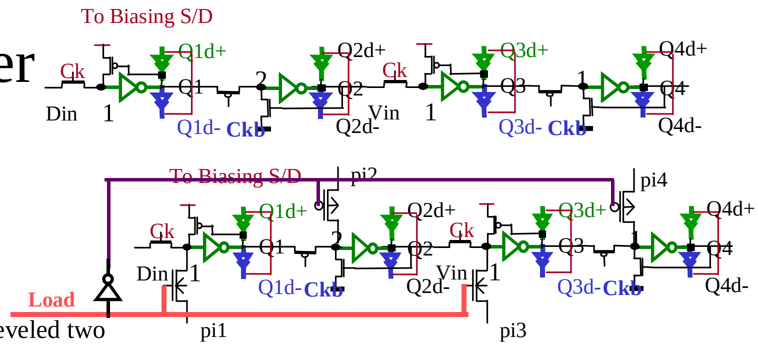
Fig. 14. SCMOS Shift Register

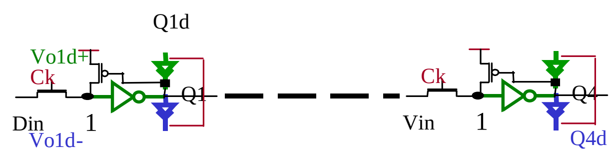
Shift Register Blocks



1.13.1 4b 4T SIPOSR

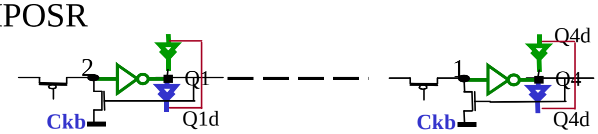
1.13.2 4b 5T PISOSR

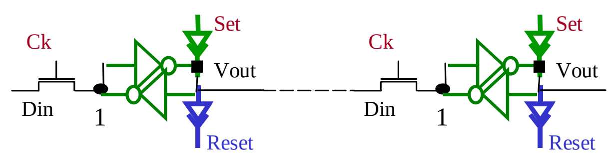
- Advanced by dc static leveled two phase clocks(**DDR, 4T per section**).
- **Universal diode output** level to biasing s/d.



1.13.3 Ck driven 4b 4T SIPOSR

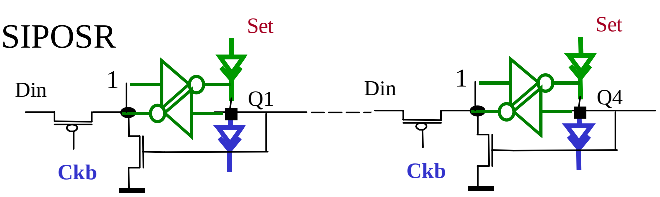
1.13.4 Ckb driven 4b 4T SIPOSR





1.13.5 Ck driven 4b 5T SIPOSR

1.13.6 Ckb driven 4b 5T SIPOSR



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Again, we found highly efficient latch and D-type flip-flop implementations. The reduction of transistor counts has significant area advantages, along with speed and power benefits for applications such as in FPGA devices, when using storage units for on-chip wiring changes.
再次，我们发现了非常有效率的门闩和 D 类型触发器。三极晶体管计数的减少有重大的面积好处，此外. 当使用此间化之门闩单元应用在于 FPGA 设备中时,在片接线之速度和功耗效益都能体现。

- **The SFPGA environment [REF. 3,4]**
- SCL 之可编程快閃列阵环境 **[**参考文 **3,4]**

Fig. 15 below illustrates the operating concept of the SCL based FPGA (SFPGA) devices and PCB subsystem, where on-chip resources form blocks that are programmable supporting various circuit configurations on the fly. Local facility includes RAM/Latches, Flash transistors, local and global wiring tracks. The PCB nets run lower speed than on-chip local bus lines. The USB2++ signal lines can be plain binary or customized to multi-level (3 or 4) to gain more bandwidth and data throughput.

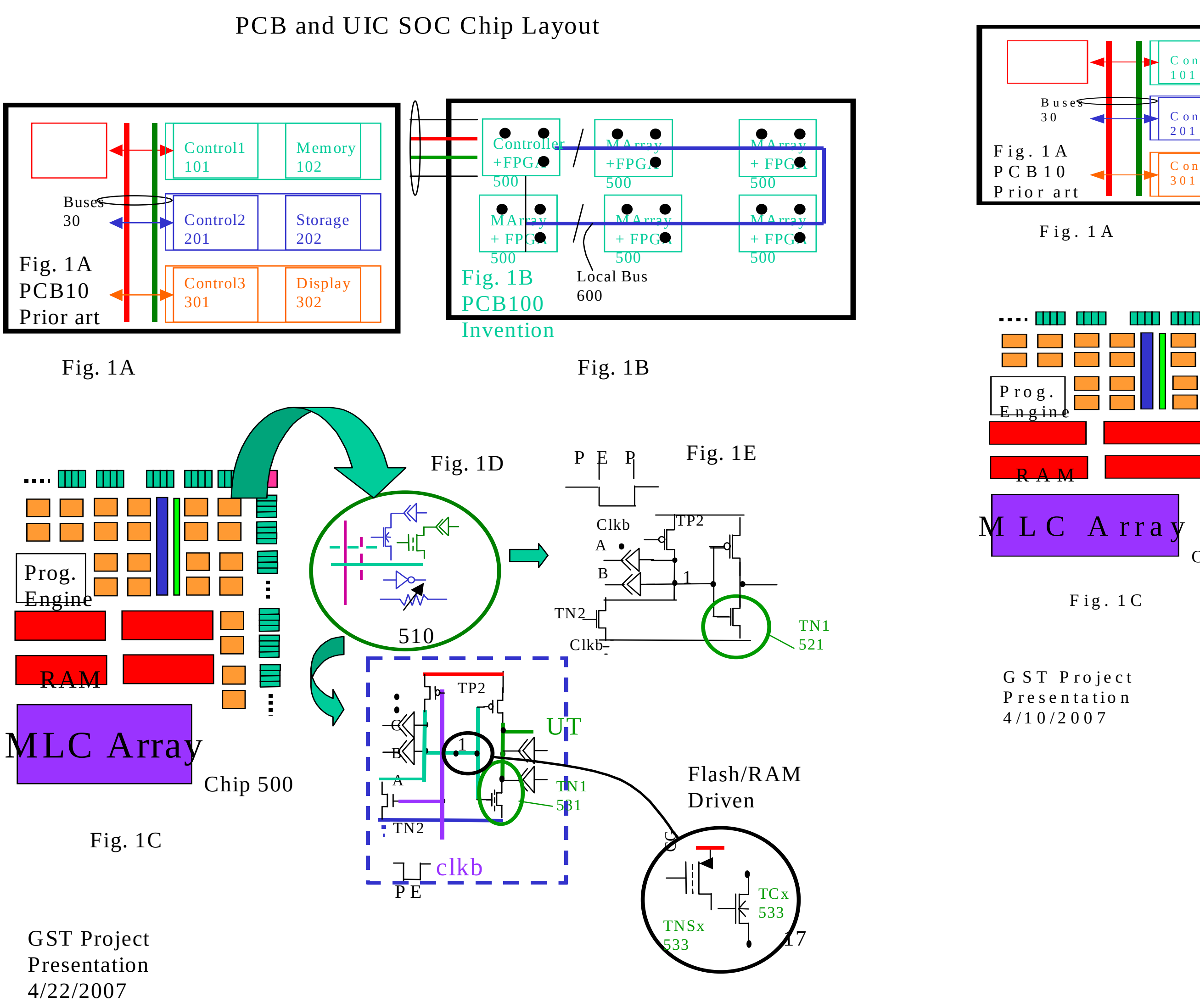
下面图 15.说明基于 SCL 之可编程快閃列阵(SFPGA) 设备,和 PCB 子系统的操作概念。在芯片上有成块的可编程序的资源,支持正在进行中各种各样的电路配置。在片地方设施包括了各类记忆体 RAM/Latches，快閃晶体管，地区性和全片性接线轨道。 PCB 排线跑的速度比在片局部排线速度慢。 USB2++之 PCB 信号线可以用简单二进制或定做多重(3 或 4) 进制, 以获取更多带宽和数据量。

Selected SCL gate may be configured as an analog comparator if the inverter transistor is swapped by a EEPROM transistor, and field programmed for single or even multiple threshold. The LtSBD offers finest granularity for voltage reference steps, since it easily divides rail-to-rail voltage drops in 100 mV steps. The signal comparison process may be multiplexed via diode channels, or pass transistor logic chain to the threshold evaluating point (the inverter input) for threshold comparison. It may yield single or even multiple bits if multiple thresholds are stored, and the bandwidth are widen.

被选的 SCL 闸门也许可配置为一或甚至多门限的比较器。如果其反相器晶体管由 EEPROM 晶体管替代, 因为 LtSBD 串可提供最精密的电压参考,每节为 100 mV, 闸门内部仅有单一网点,我们能容易地划分并调控比较三极管障压之下落轨迹。信号比较过程也可经由二极管渠道或者通道晶体管逻辑链,对多门限评估点(反相器的输入)做门限比较。 如果存放过程为单一或多门限，每次解玛可产生唯一甚至多位比特,增多带宽和数据量。

Fig. 15, SCMOS FPGA PCB environment

图 15. SCL 之可编程快閃列阵设备,和 PCB 子系统

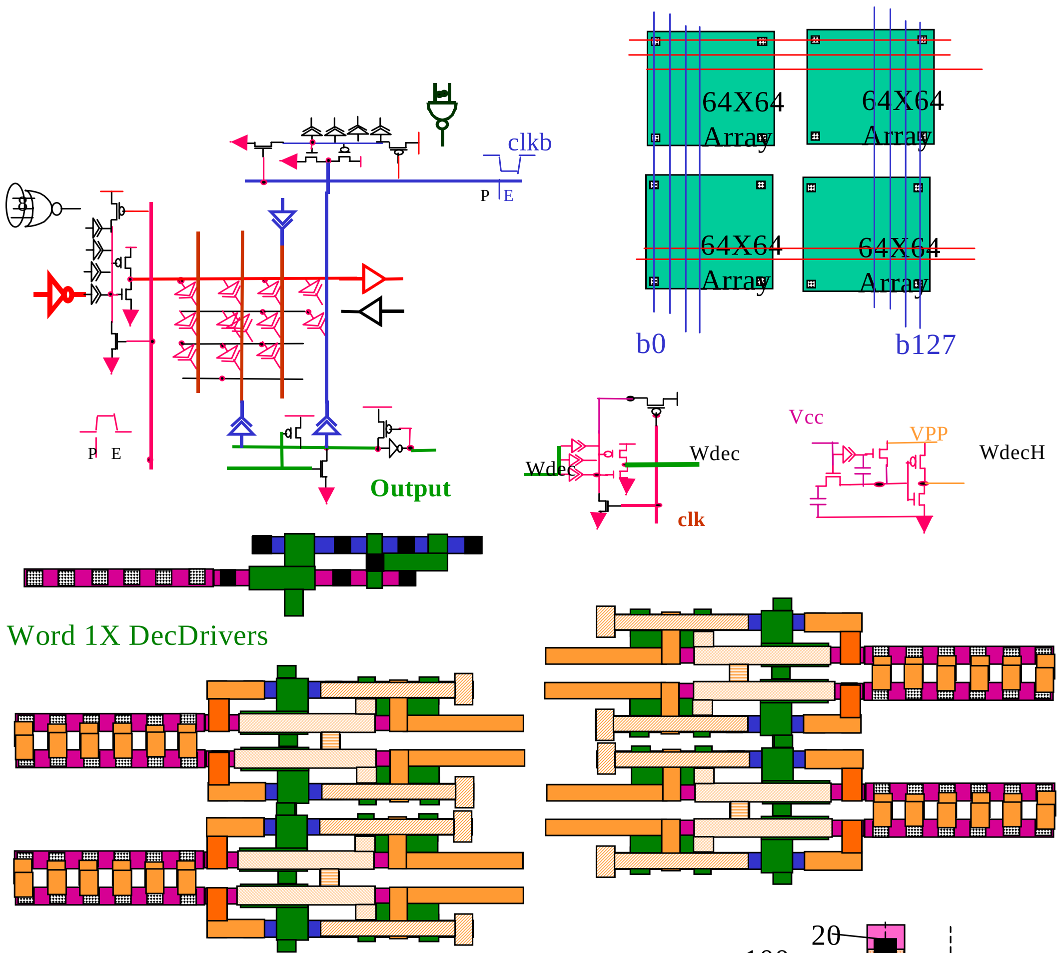


- The SBD Array Core Design
- 肖特基列阵之核心设计

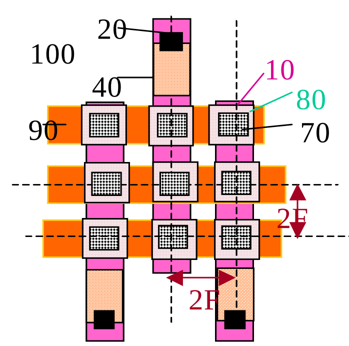
Fig. 16 below shows the SBD array core layout, with array on 4F^2/bit packing grids. The Word Line decoders also fit nicely to 2F pitch grids driving array diodes in E-W and opposite directions (W-E). In Fig. 16, The 256 word decoder M1word lines feeds horizontally(X-Axis, and symmetrically (Y-Axis.

下面图 16. 显示 SBD 列阵核心布局, 以 4F^2/bit 为列阵包装栅格。列阵之字线译码器恰好也适合到 2F 栅格, 驱动由二极管和相反向器组合之译码器和字线在东西向行走。 在图 16 里，256 条 M1 排线和译码器以水平 XY 轴-走向对称布局。

Fig. 16, Word Decode and Word line layout schematics
图 16. 列阵之核心设计,字解码, 字驱动



GSD Semiconductor NV OTP Memory Density Chart						
	Mb/cm^2	cell efficiency				
F in um	1/4F^2	0.9	0.8	0.7	0.6	0.5
0.25	400	360	320	280	240	200
0.18	816	735	653	571	490	408
0.12	1666	1499	1333	1166	1000	833
0.09	3400	3060	2720	2380	2040	1700
0.06	6939	6245	5551	4857	4163	3469



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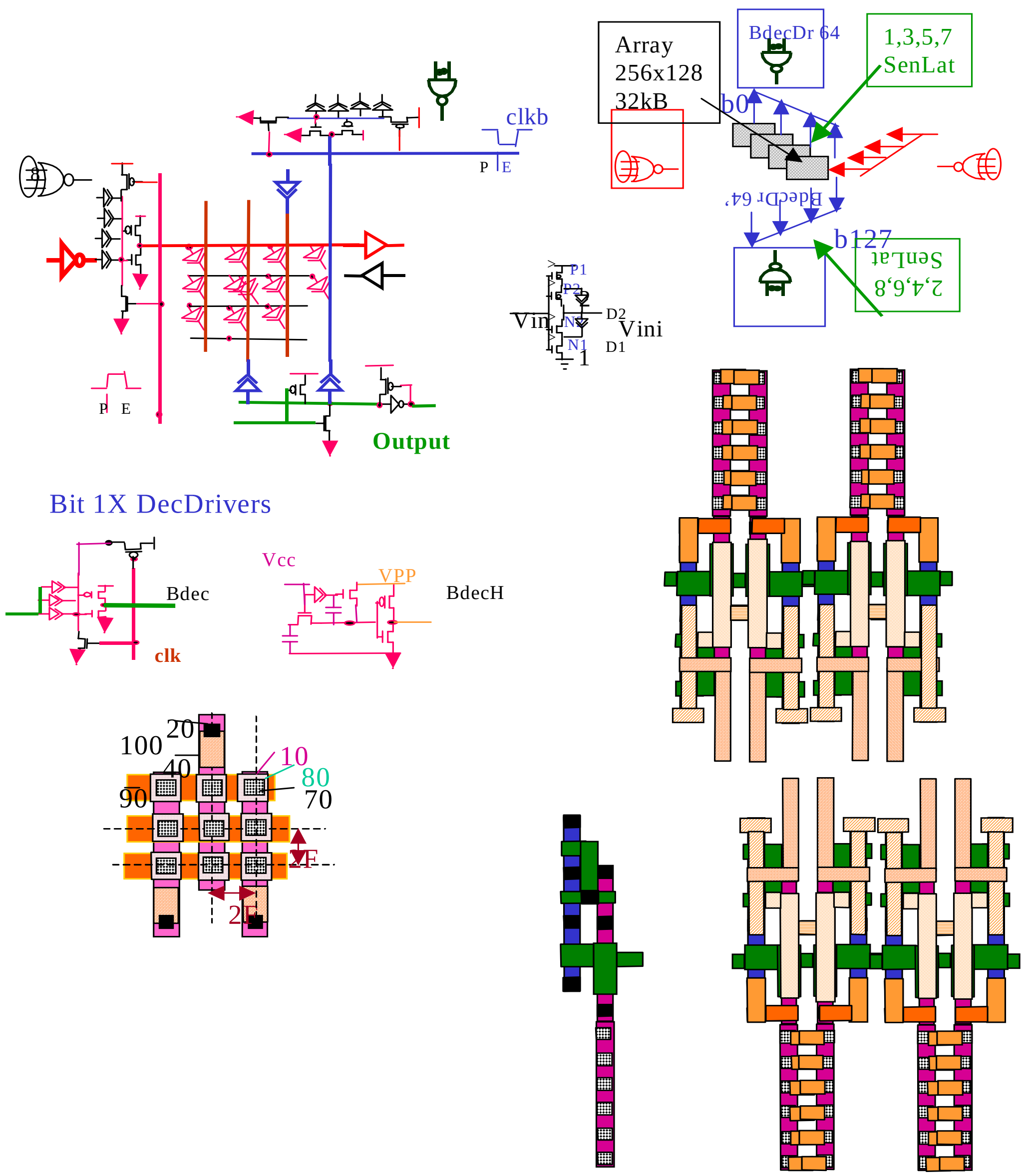
In Fig. 17 below, the array bit lines (128) run vertically with diffusion path shortened from top by M2 metal stitches. The array selects 256x128 (32k) codes and output 1-bit. 8 planes(copies) of arrays will yield 32KX8 high speed ROM for 1 ns cycle time, and read out program/data, 2 Byte/2 phase.

在下面图 17，列阵点线(128)用 M2 金属从上面缩减短垂直方向的扩散道路电阻。 列阵选择 256x128 (32k) 解码和 1 位输出。 8 层平面(拷贝)列阵将产生 32KX8 高速 ROM。 以 1 奈秒 ns 周期,分 2 阶段读出 2 Byte 之程序或者数据。



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- **The embedded memory unit**
- 嵌入式记忆体

The embedded memory arrays include high density, high speed Mask ROM, OTP (One-time-Programmable) ROM, SRAM, DRAM, EEPROM, single-level-cell (SLC) Flash, and multi-level-cell (MLC) Flash entities. Flash device is denser than DRAM but is slow. The LtSBD may serve in the core array cells as in the case of 6TSRAM[REF. 1,2], Mask ROM, and OTP ROM macros. The latter two implementations shall realize triple benefits; densest arrays (basically low cost processes and being single contact/bit), fast speed, and low power consumption

嵌入式记忆列阵包括高密度，高速之光罩编程的点阵记忆体(Mask ROM)、一次性可编程序记忆体 (OTP ROM)、静忒记忆体 SRAM、动忒记忆体 DRAM、电子更改记忆体 EEPROM、单一狀忒(二层次) 快閃晶体管 (SLC), 和多层次快閃晶体管(MLC)。快閃设备比动忒记忆体密集，但是太慢。低障肖特基管 LtSBD 可作为核心矩阵服务,取代傳統之 6TSRAM [参考文 1,2]、Mask ROM 和 OTP ROM 等宏指令库。 后二者实施将体现三倍好处;基本上便宜的制程, 快速, 和低功耗。

- **Wide piggy bag benefits to all memory and processor devices**

- 各类记忆体及处理机之外快好处

The SCL peripherals may also be employed to enhance array (DRAM, Flash) performance; gaining speed, density, and power efficiency. Classes of the Memory speeds ranked from SRAM (nS), DRAM (10s of nS), ROM (100s of nS), to Flash (a few uS) and hard disk (mS) while storage areas rank to the opposite direction. Normally, transistor ROMs (and EEPROM/Flash devices) were considerably slower than RAMs. However, due to area reduction, fast SBD circuits, and Vsupply reduction, the **SCMOS ROMs, and SCL wrapped** DRAM (Psuedo SRAM), and Flash arrays, 4T-SRAM **shall claim all advantages one can ever dream of.**

SCL 外围设备也可使用于各种列阵(动忒记忆体，快閃电路), 提高功能;获取速度、密度和提升功耗效率。各类记忆体之速度依次为 SRAM 奈秒级(nS)， DRAM10 奈秒级(10 nS)， ROM，Flash 微秒级(uS)，而贮存密度去反向正好相反。 通常，三极管 ROMs (加上 EEPROM/Flash 设备) 比(SRAM/DRAM)可观地慢。 然而，由于实际面积减少、快速的 SBD 电路, 和 Vsupply 降低、SCMOS ROMs 和 SCL 包裹后的 DRAM, Psuedo 6TSRAM 电路，SCL 包裹后的 快閃电路， 和由 SCMOS 做的 4T-SRAM 将能达到你可能梦想的所有好处。

SBD ROM may have huge on-chip control store and fast cycle times for fast state machine in search engines for BIOS routines, games/DNA codes, Letter, Image, and Audio storages, and BIST (build-in-sef-test) programs. It may replace functions of conventional SRAM (near nS) and exceed conventional DRAM (10s of nS), and Flash devices (uS) in power-speed and cost considerations

SBD 光罩编程记忆体 ROM 具大量的内存,及快速之在片读出周期, 可用之于处理机之基本系统操作码, 游戏机控制码, 文字图画音像储存, 基因識別码, 内存测试码修造自备测试 (BIST). 在速度功耗和成本的考量上, 它们可以取代那些常规 6T 静忒记忆体 SRAM(奈秒级 nS), 并超越常规的动忒记忆 DRAM(10s of nS), 和快閃电路 Flash (微秒 uS) 设备。

The SCMOS chips shall continue Moore's law with improved DTL circuit topology and simplified SCL circuits, which are without the expensive and stacked TTL legs; all CMOS TTL nets with more than 2 way input gates are replaced. Thus, supply voltage and on/off chip signal swings may be substantially lowered, and one can expect all the nice features (density, speed, power, and field programmability) with the emerging SCMOS implementations

SCMOS 芯片用被改进的 DTL 电路拓扑结构和被简化的 SCL 电路，将继推动续摩尔定律。它没有昂贵和堆积的 TTL 大腿; 所有 CMOS TTL 网中, 凡是超过 2 位输入门的闸门都被替换。 因此，电源电压，在片和离片信号振幅均被下降。你可能期望所有好的特点(密度、速度、功耗、面积、良率和可编程序性)都涌现于 SCMOS 的实施中。

The SCMOS Technology and Applications-an integrated circuit white paper.
A.W.Chang, June, 2007

The SCMOS solution shall offer a powerful design platform for the 5th generation microchips. We have opened new practices that diodes replace transistors as the massive switching elements and core arrays, and the dynamical low power nets manage efficiently over-all chip power consumptions, and multi-level, in addition to binary computing, starts with the finest diode threshold divisions for the analog voltage drops.

SCMOS 解答方案将提供一个强有力的设计平台, 开发第 5 世代微电子集成电路产品。 我们打开了新的实践,以二极管替换三极晶体管作为巨型的开关元素和核心列阵，并且动态低功耗网有效地处理整体芯片之电力消费。除二进制计算之外，加上多重进制计算，开始以最精细的二极管门限划分类比电压。

The SCMOS drives with ease physical size and electrical signal scale-downs, setting new records and trends for low power, high performance microelectronics on a new chapter. And I believe it shall emerge, after copper conductor and Flash technology, as the new tramp cards for mainstream SoC solutions. It shall serve as vital alternatives to continue Moore’s law with CMOS TTL. Leaders in world class foundries and IP developers ought to seriously consider it for generic applications, special payoff is expected for personal mobile communication and multi-level signal processing.

SCMOS 在一个新的章节里, 容易地驱动物理尺寸和电信信号小下来，设置新纪录和趋向，推进低功耗，高性能微电子产业。 并且我相信它能在继铜导线和快閃技术之后涌现大量实施，作为新的王牌成为主流单一芯片 SoC 机之解答。 它将担当重要任务,在 CMOS TTL 之后继续摩尔定律。凡具有国际水平的流片厂和 IP 开发商之高层领导, 应该慎重考虑它, 作为普通应用。个人移动式通信,和多重信号处理业者, 更应有特别期望。

5. Summary and Conclusion
5. 摘要和结论

1. **We have demonstrated the theory and data points of a newly invented diode element-LtSBD for next generation IC.**

1. 我们展示了一个最新被发明的二极管元素 LtSBD 的理论和数据点，为下一代集成电路。

2. **The LtSBD supports a new class of IC technology-SCMOS, which exhibits excellent attributes for low power, high performance product applications.**

2. LtSBD 支持新的集成电路技术 SCMOS，陈列优秀属性,能为低功率，高性能产品应用。

3. **Broad ALM macro functions are created in the initial SCMOS design libraries.**

3. 创造设计了初步的类比,逻辑,记忆体功能的宏指令集 ALM MACRO。

4. **The SCMOS devices are unique and revolutionary in theory and concept, and far more efficient than the present CMOS state-of-the-arts solutions. The benefit matrices are Capacity, Speed, Power Saving, Cost and Service Conveniences. We welcome investors and partners.**

4. 超级 CMOS 工艺在理论和概念上具独特和革命性,比现有的 CMOS 工艺更加高效率。具体优势是容量、速度、能源节约、费用和服务便利。我们欢迎投资者和伙伴。

5. **The SCL may be employed in many product embodiments. They replace existing arts in microelectronics designs, support mixed signal SoC integrations with embedded units.**

5. **SCL** 能在许多产品中被使用。他们能以嵌入单位**,** 取代现有微电子设计**,**支持混合信号**,**单一芯片系统 **SoC** 综合化。

6. **SCMOS allows users to explore new horizons with open vision and sets no limits. The technology can port to any foundries lines（3-12 IN Si Wafer）and system clients.**

6. 超级 CMOS 让用户探索新天地，并不设限。该 技术可于各代（3-12 寸晶圆片）流片厂工艺接軌。

7. **SCMOS is the way to go for the next decades. It is the answer to push the Moore's rule further.**

7. 超级 CMOS 适用于下十年。 它是进一步推动摩尔规则的答案。

6. References

6. 参考

Two US core patents were granted for SCMOS circuits and methods. (For patent research please click www.uspto.org)

SCMOS 电路和方法被授予了二个美国核心专利。 (专利研究请点击 www.uspto.org)

1. US Pat. 6,852,578 - Filed January 15, 2003, and
美国专利。 6,852,578 - 2003 年 1 月 15 日归档，和
2. US Pat. 6,590,800 - Filed June 15, 2001
美国专利。 6,590,800 - 2001 年 6 月 15 日归档

Two children patents on Flash techniques were filed and granted.
并且被授予在快闪技术二个衍生专利归档了。

3. SCL type FPGA with multi-threshold transistors and method for forming same

US Pat. 7,135,890 - Filed April 19, 2004 - Super Talent Electronics, Inc.

美国专利. 7,135,890 - 2004 年 4 月 19 日归档-超级天才电子公司

4. Flash memory device and architecture with multi level cells
US Pat. 7,082,056 - Filed March 12, 2004 - Super Talent Electronics, Inc.

美国专利. 7,082,056 - 2004 年 3 月 12 日归档-超级天才电子公司

Many proliferated ASIC/generic applications are in areas of RAM and ROM, SLC/MLS Flash devices, analog, and wired/wireless infra-structural implementations. Many chip process, hardware, and software means for multi-level computing are claimed

许多专用集成电路 ASIC/generic 应用于 RAM 和 ROM， SLC/MLS 快闪设备、类比、和有线或无线基础建设实施领域。 许多芯片制程，硬件，多重计算之软件手段已在审批。

